X1210 Mono Disk Drive Unit

Volume 3 - Device Logic (First Draft)

ERRATUM

The following errors are present in this first draft:

Page	Para	Line	Error
4	3	3	Signal $\overline{CIP}^*$ and $\overline{CIE}_*$ should be $\overline{CIP*}$ and $\overline{CIE*}$
9	2	3	'energies should be energises
16	4	4	'hte' should be the
18	3 (c)	2	insert word'to' between'through' and 'the'.
20	7	1	'cantridge'should be cartridge.
22	5	2	change IV to 1V.
29	3	5	change ov to 0V.
30	1	4	change 'positive' to negative.
30	1	5	insert the word negative between words 'the' and 'voltage'.
40	5	7	change 'ninth' to eighth.
44	2	7	change 'move' to more.
49	5	2	change '16' to 15.
59	4	2	add an 's' to word prevent

ILLUSTRATIONS

It is intended that figs 3.29 and 3.30 be made into'facing pages' in order that the circuit and waveforms of a greater than 16 steps seek can be viewed simultaneously. Thus in the 2nd draft, fig. 3.30 will be made into a left hand page and re-numbered fig. 3.29. Fig. 3.29 will be re-numbered 3.30 accordingly.
Annotation on retract micro-switch on Fig. 3.15
'held on by positioner'should be held open by positioner.

Fig. 3.35 arrow leaders from PMEP'and H0D' to R' should go to RTRP'.

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INTRODUCTION

The principle functions performed by the logic are discussed briefly as follows:

Safety Control - Operator actions associated with the cartridge loading sequence are checked by the logic. If an incorrect step is implemented during this sequence, the logic prevents the X1210 from starting. Furthermore, safety logic inherent in the machine ensures that the operational conditions necessary to maintain the integrity of this disc memory are satisfied during all instants of operation.

Cleaning Control - The logic commands complete control of the cleaning cycle.

Position Control - Address instructions issued by the control unit are interpreted by the logic in order to guide the positioning mechanism to the required track of the magnetic disk.

Head Selection - The head select instructions issued by the control unit are interpreted in order that either the upper or the lower read-write head is energised.

THE POSITIONING MECHANISM

Brief Description

The positioning mechanism comprises an electrical stepping motor coupled by a rack and pinion to a carriage mounted on two parallel guide rails. The front of the carriage supports the two read-write heads.

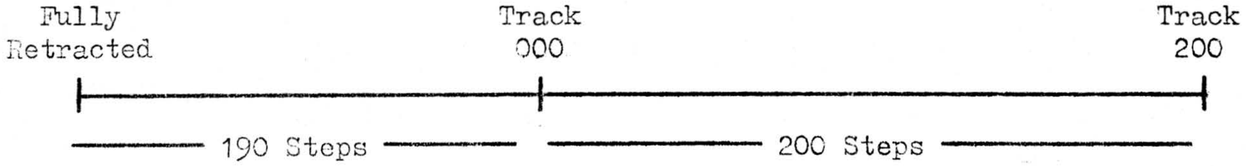


Fig. 3.1 - The Limits of Travel

The limits of travel of the positioning mechanism are illustrated in Fig. 3.1. When the X1210 has been stopped, the logic automatically moves the positioning mechanism to the fully retracted position. In this position, the read-write heads are completely withdrawn from the cartridge thus permitting cartridge exchange.

The fully retracted position is defined by a micro-switch.

When it is in this position it maintains the switch open. The 'retracted' micro-switch thus serves as a sensor informing the logic when the positioner is fully retracted.

When the X1210 is started, the logic guides the positioning mechanism forward and inserts the read-write heads into the cartridge. During this forward stroke the nylon cleaning brushes in the heads are held in contact with the magnetic disk whilst the read-write assemblies are kept retracted within the heads. At the end of this forward stroke, the positioning mechanism opens a micro-switch stationed at track 200. When this occurs, the logic reverses the positioning mechanism back towards track 000. And at the same time, it terminates the cleaning cycle by lifting the brushes from the magnetic disc and loads the read-write heads into the flying position.

Each of the tracks on the magnetic disk are radially spaced at 262µ meters. When all the relevant production tolerances and dimensional changes due to temperature variation are accounted for, the alignment tolerance of the positioning mechanism about each track has been conservatively estimated to be about 40µ metres. Each discrete step movement performed by the positioning mechanism equals the track-to-track distance. Thus the distance from track 000 to track 200 can be expressed as 200 steps.

CONTROL OF THE POSITIONING MECHANISM

To appreciate the relationship between the condition of the logic and the physical position of the positioning mechanism, it is necessary to have a clear understanding of their interface - the stepping motor.

The Stepping Motor Basic Principle

Fig. 3.2 illustrates the principle diagrammatically. The motor illustrated is a simpler version than that used on the X1210.

It is a four phase, two pole type; this means that the stator has four windings and the rotor two poles (one pole pair).

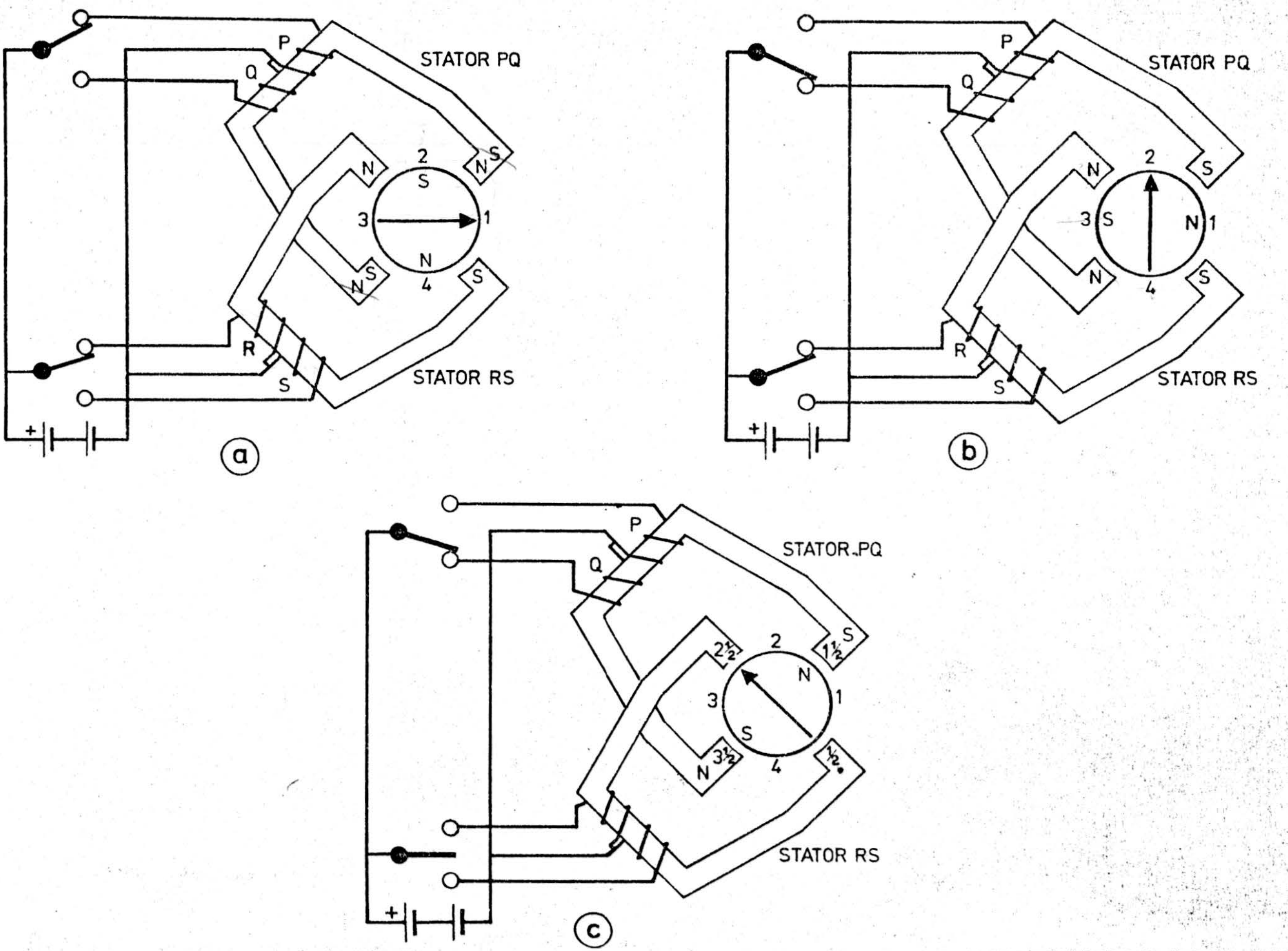


Fig. 3.2 - Diagrammatic Representation of a 4 phase, 2 pole Motor.

With windings P and R energised, the four stator poles take the polarity shown in (a) and the rotor turns to step position 1. If winding Q is now energised instead of P, the rotor will turn 90° anti-clockwise to step position 2 shown in (b). Steps 3 and 4 can be obtained in a similar fashion. Fig. 3.2 (c) shows the effect of completely de-energising the windings R and S. The rotor turns by only half a step to step position $2\frac{1}{2}$. Similarly, if winding P and Q had been completely de-energised, the rotor would have turned anti-clockwise to position $1\frac{1}{2}$.

Clearly then, by energising and de-energising the windings of this motor in a 2 : 1 : 2 sequence, double the number of discrete rotor positions are available.

The X1210 Stepping Motor

The stepping motor used on the X1210 is an 4 phase, 24 pole type. The same principle of sequentially energising the windings is applied to this motor in order to increase its angular resolution - and thus also the linear resolution of the positioning mechanism.

The construction of the motor is best described in relation to fig. 3.3 which shows exactly half of the rotor and stator and all of the control windings. The eight windings are grouped into four groups of two: A, B, C and D. Each pair of coils forming a winding - say for example pair A - are wound around twelve equally distributed stator pole pieces. It can also be seen in the diagram each of the twelve pole pieces form one of a group of four pole pieces. The other pole pieces in the group being controlled similarly by control windings B, C and D. Each group of four pole pieces corresponds to a span of one rotor pole pair.

Each pole piece can be set to three distinct states - along with its eleven other associated pole pieces. Consider for example all those controlled by winding A. Energising coil $\overline{\text{CIP}}$ *, $\overline{\text{CIE}}$ * would set the twelve associated pole pieces to identical polarities. If now this coil is de-energised and coil C2P *, $\overline{\text{C2E}}$ * is energised instead, the polarity of each of these pole pieces would be reversed. The third state is achieved by completely de-energising both coils of winding A. In this condition each of the associated pole pieces can be considered to possess no polarity whatsoever, ie they have negligible residual magnetism.

The angular resolution of the stepping motor is increased by energising the four pairs of control windings A, B, C and D in a 4 : 3 : 4 sequence. This is illustrated in fig. 3.4. The diagram shows the polarity of each stator pole tip as set by the condition of its control winding. The state of each winding is shown in the 'Energised'column. The absence of the winding reference indicates that both coils forming the winding are de-energised.

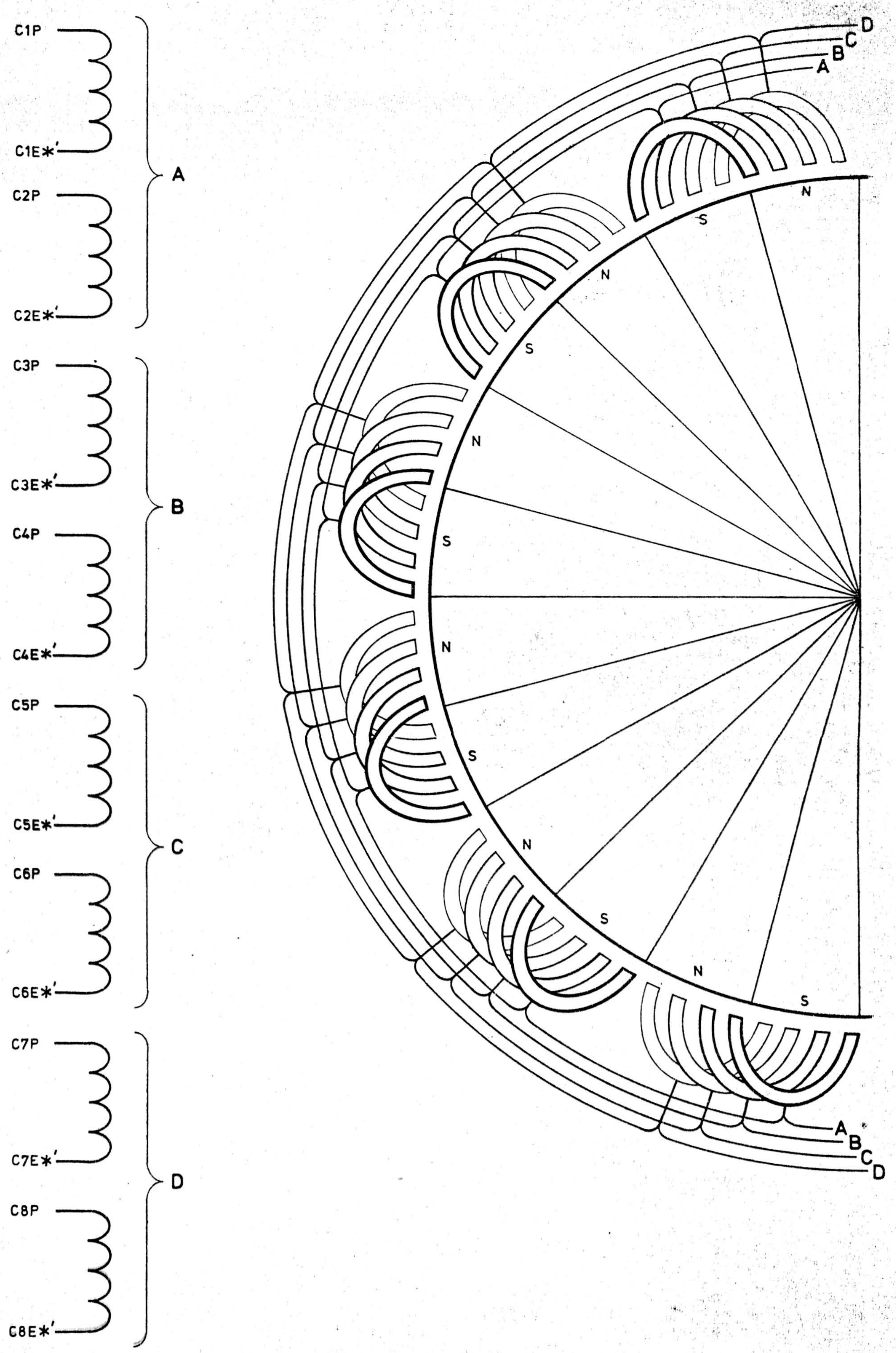
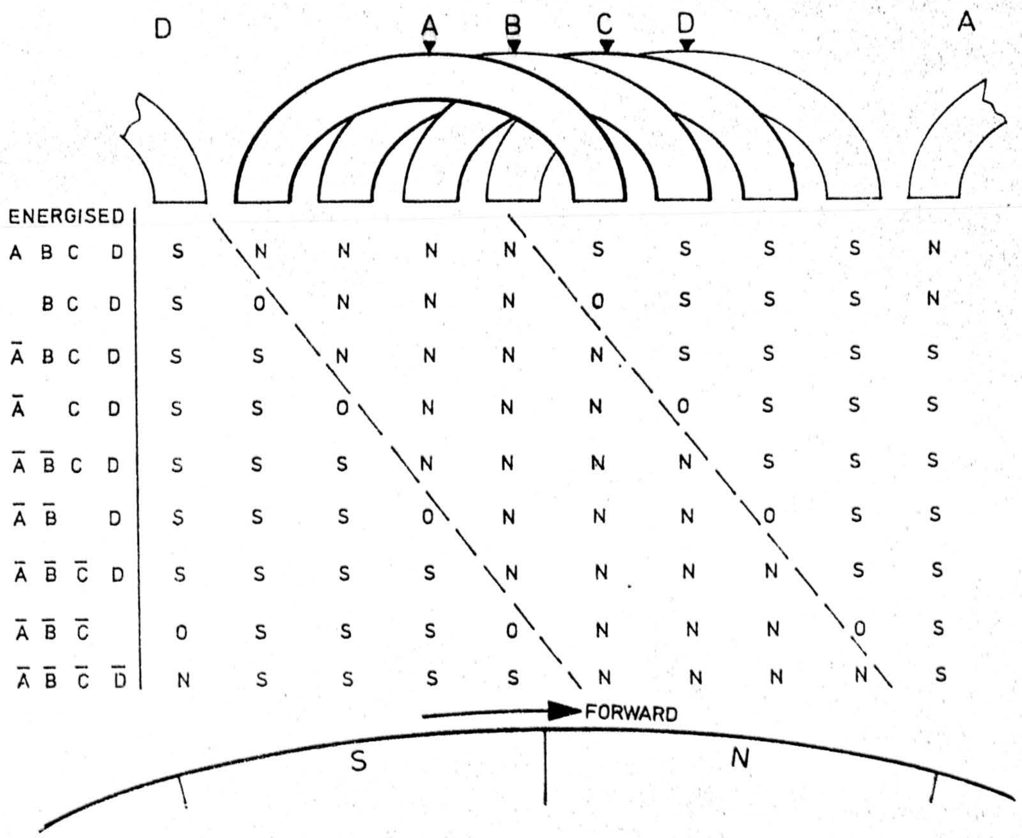


Fig. 3.3 The X1210 Stepping Motor.



ENERGISED										
A B C D	S	N	N	N	N	S	S	S	S	N
B C D	S	0	N	N	N	0	S	S	S	N
$\bar{A}$ B C D	S	S	N	N	N	N	S	S	S	S
$\bar{A}$ C D	S	S	0	N	N	N	0	S	S	S
$\bar{A}$ $\bar{B}$ C D	S	S	S	N	N	N	N	S	S	S
$\bar{A}$ $\bar{B}$ D	S	S	S	0	N	N	N	0	S	S
$\bar{A}$ $\bar{B}$ $\bar{C}$ D	S	S	S	S	N	N	N	N	S	S
$\bar{A}$ $\bar{B}$ $\bar{C}$	0	S	S	S	0	N	N	N	0	S
$\bar{A}$ $\bar{B}$ $\bar{C}$ $\bar{D}$	N	S	S	S	S	N	N	N	N	S

Fig. 3.4 Pole Polarities Set by Control Windings.

In line 1, assume one coil in each of the four control windings A, B, C and D is energised giving the stator poles the polarity shown. The rotor pole pair will thus align itself as shown. The rotor south polarity aligning itself at a point, midway between the pole tips of B and C.

If winding A is now completely de-energised the pole tips controlled by A will lose their polarity. This will cause the resultant point of the stator magnetic field to shift to the right - as is shown in line 2. The rotor poles will thus shift to the right by 1 step and align themselves with the pole tips controlled by winding C. In line 3, the first coil is maintained de-energised. Instead the other coil of A is energised. This is indicated by placing a bar over the letter. Hence $\bar{A}$. In this condition, the polarity of the poles controlled by A is now reversed in relation to its original condition in line 1. This again has the same effect. The resultant point of the stator magnetic field is shifted to the right by the same amount as before. The rotor thus rotates 1 step to the right aligning itself midway between the pole tips of C and D.

If this process were continued until the energised condition of the coils is that shown in line 9 $(\overline{A},\overline{B},\overline{C},\overline{D})$, the rotor south pole will have moved by a total of eight steps until it is aligned midway between the tips of B and C.
The energising sequence of 4 : 3 : 4 is clearly shown in the 'Energised' column of Fig 3.4.

Control of The Stepping Motor

Control of the stepping motor is effected by the decoding logic on card 8. This logic consists essentially of a reversible 4-bit counter termed the binary up/down counter and two binary-to-octal decoders. The function of this circuit is to transform a stream of clock pulses into a parallel octal code that will enable the stepping motor control windings to be energised in the required 4 : 3 : 4 sequence.

This logic is almost completely described by its truth table which has been combined with the essential section of the decoding logic on Fig. 3.5.

The decoding logic can be considered to have three inputs. These are the variable clock input SMCCP. Signal $\overline{\text{SMCUP}}$ which controlles the cyclic rotation of the counter. And signal $\overline{\text{SKCF}}$. This latter signal controls the outputs gates of the decoding logic.

When a seek mission is initiated, the logic selects a particular clock source of fixed frequency and feeds it on the variable clock input, SMCCP, to the trigger input of the binary up/down counter. The frequency selected by the logic is dependant upon the size of the seek mission. If $\overline{\text{SMCUP}}$ is logic 1, the up/down counter proceeds through the binary progression states in the direction 0000 to 1111 at a counting rate equivalent to the variable clock frequency.

Each of the up/down counters 1-2-4-8 columns are fed to the inputs of the binary-to-octal decoders. Column 1 is fed on line SMCA; column 2 on SMCB and so on.

The effects of feeding the contents of each of the counters four columns to the binary-to-octal decoders is shown in the truth table. When the counter is at state 0000, the output pin 0 of both decoders H and I are set to logic 0. After one variable clock pulse is fed into the counter its state (0001) causes pin 0 of decoder I to become logic 1

Pin 0 of decoder H remains at logic 0 however. As the count proceeds towards 1111, logic 0 is moved in turn from pin 1 towards pin 7 on the outputs of each decoder. When after fifteen variable clock pulses have been fed into the counter its state becomes 1111. It can be seen from the truth table that pins 1 to 7 of decoder I are all at logic 1 under these conditions. But pin 7 of decoder H is at logic 0. On the sixteenth variable clock pulse the up/down counter resets to the zero state (0000) and commences counting again towards the state 1111. This cycling of the counter continues until the variable clock frequency is stopped.

As the logic 0 progresses from pin 0 to pin 7 on the outputs of each decoder during the count cycle, its effect on the outputs to the stepping motor control windings can be established by examination of the circuit and its truth table.

When the condition of the up/down counter is 0000 pin 0 on each decoder is at logic 0. Thus both $\overline{\mathrm{1S00}}$ and $\overline{\mathrm{2S0001}}$ are set to logic 0. $\overline{\mathrm{1S00}}$ sets CD8P to logic 1. And $\overline{\mathrm{2S0001}}$ sets CD6P to logic 1. When a seek mission has been initiated signal $\overline{\mathrm{SKCF}}$ is set to logic 1 and enables the output gates of the decoding logic. $\overline{\mathrm{SKCF}}$ (=1) and CP8P (=1) sets $\overline{\mathrm{CD8E}}$ to logic 0. Whilst $\overline{\mathrm{SKCF}}$ (=1) and CD6P (=1) sets $\overline{\mathrm{CD6E}}$ to logic 0. Signal $\overline{\mathrm{4S0003}}$ is also set to logic 0 by the state of the up/down counter. This signal sets both CD2P and CD4P to logic 1 causing CD2E and $\overline{\mathrm{CD4E}}$ to be set to zero. Thus signals $\overline{\mathrm{CD2E}}$, $\overline{\mathrm{CD4E}}$, $\overline{\mathrm{CD6E}}$ and $\overline{\mathrm{CD8E}}$ have all been set to zero by the cleared state of the counter. Each of these signals is applied via a coil driver amplifier to one of the eight coils of the stepping motor. The operation of each coil driver amplifier is identical.

If for example $\overline{\mathrm{CD1E}}$ becomes 0, the base of transistor TS1 of the coil driver is forward biased driving TS1 into the conduction region. The base of TS2 is therefore forward biased by the collector current voltage drop across resistor R4. This causes TS2 to be bottomed, completing a circuit from the 24v dc supply via R5 and the relevant stepping motor coil. Thus since four of the coil driver inputs have been set to logic 0, four of the stepping motor coils will be energised.

If this whole procedure is repeated one variable clock pulse later, the state of the counter will be 0001. Line 2 of the truth table shows the logical conditions at the input to the coil driver amplifiers for this condition. And it can be seen that $\overline{\mathrm{CD2E}}$, $\overline{\mathrm{CD4E}}$ and $\overline{\mathrm{CD6E}}$ are at logic 0. Thus one of the four coils originally energised has now been de-energised leaving only three in the energised state.

Line 3 of the truth table shows the logical condition at the input to the coil drivers when two variable clock pulses have been fed into the counter (0010). And it can be seen that $\overline{\text{CD2E}}$, $\overline{\text{CD4E}}$, $\overline{\text{CD6E}}$ and $\overline{\text{CD7E}}$ are at logic 0. Once again four of the stepping motor coils are in the energised state.

If this procedure is continued throughout one complete binary count cycle of the up/down counter, it is clear by inspection of the truth table that the decoding logic energies and de-energises the stepping motor coils in the required 4 : 3 : 4 sequence discussed earlier.

When $\overline{\text{SMCUP}}$ is logic 1 - as has been assumed in this discussion - the direction of rotation of the stepping motor is in the forward direction. Conversely, when $\overline{\text{SMCUP}}$ is logic 0, the cyclic rotation of the counter is reversed it counts down from 1111 to 0000. Under these conditions the stepping motor rotation is reversed. This drives the positioning mechanism in the reverse direction (towards track 000).

At the appropriate instant at the end of a seek mission $\overline{\text{SKCF}}$ is set to logic 0. This causes the inputs to the coil driver amplifiers to be set to 1, switching off the transistors and resulting in all the stepping motor coils being de-energised.

THE LOGIC-POSITIONING MECHANISM RELATIONSHIP

The positioning mechanism is set up such that when the read-write heads are aligned over track 000, the condition of the binary up/down counter is 0000.

If the positioner is at track 000 and a seek mission is initiated, when sixteen variable clock pulses have been fed into the up/down counter. It will have counted from 0000 to 1111 and reset to 0000 again. At the same time, the positioning mechanism will have moved by sixteen tracks of the disk. Thus the cleared condition (0000) of the up/down counter will be repeated at track sixteen and at all positions that are multiples of sixteen steps from track 000. This will apply whether the positioning mechanism moves either forward or reverse.

The Fully Retracted Position

If the dc supply is removed from the up/down counter and then re-applied, there is only a 1 in 16 chance that its logical condition will correspond to that condition prior to removal of the supplies.

Despite this fact, the relationship between the logic and the physical position of the positioning mechanism remains unaffected.

This is particularly relevant when the positioning mechanism is fully retracted. Since it is normally in this position when the power supplies are switched off.

If the number of steps between track 000 and the retracted micro-switch were an exact multiple of 16, the condition of the up/down counter at the instant of opening the retract micro-switch would be 0000. And since the positioning mechanism stops the instant this switch is opened, the final condition of the counter would be 0000. And the positioning mechanism would be stationed at an exact multiple of 16 steps from track 000.

Suppose now that the X1210 power supplies were switched off and then switched on again. The new condition of the up/down counter could be anywhere from 0000 to 1111. If the new condition were 1111, the position of the rotor poles would only be 1 step from the new position of the stator poles. The positioning mechanism would thus shift by by 1 step to the new position. The direction of this step would be towards the retracted position.

If however the new condition of the counter were eight steps from condition 0000 (1000) the stator poles would shift by eight steps. The rotor poles would thus be adjacent stator poles of the same polarity as is shown below.

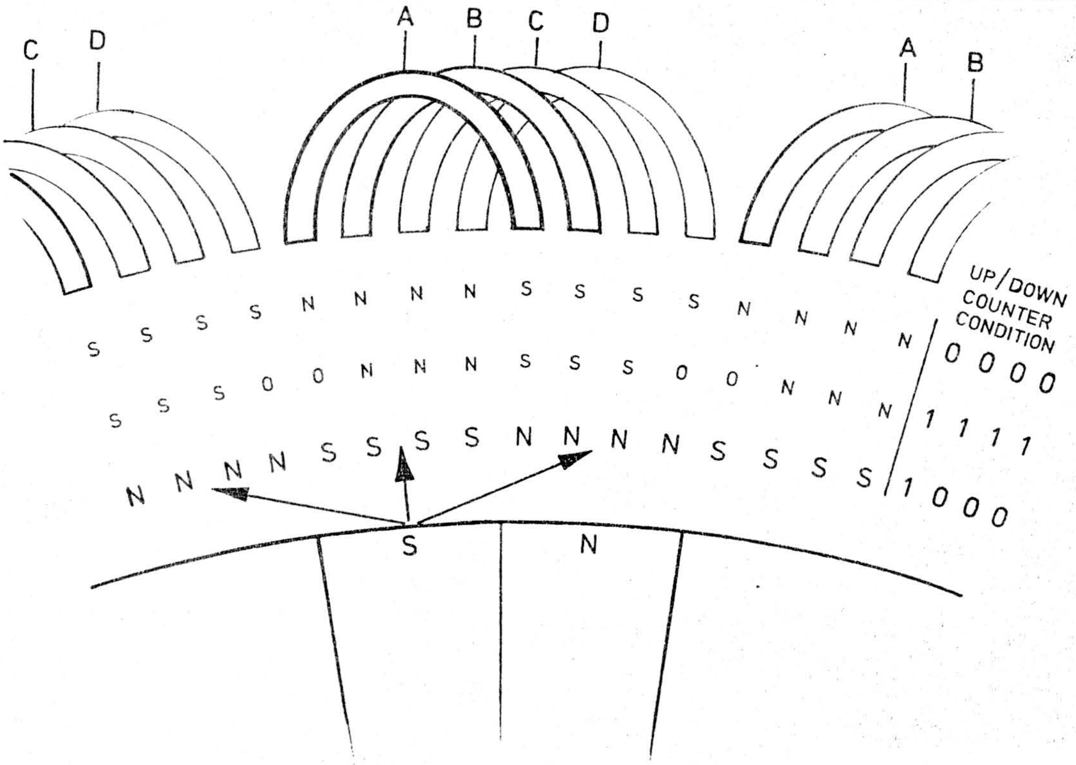


Fig. 3.6 The Rotor Stable States.

This diagram illustrates the pole polarities for the conditions 0000, 1111 and 1000 of the up/down counter. In the condition 1000, there are three possible stable states of the rotor. It could remain locked opposite the stator poles of the same polarity, midway between the two attacting stator poles of opposite polarity. It is highly unlikely though that a state of equilibrium in this position would be maintained if the positioner accelerated from rest due to friction and inertia. And thus it will be dis-regarded. The two other stable states are obtainable if the rotor shifts either to the right and aligns midway between the four poles of opposite polarity or similarly to the left. Each of these stable positions are exactly 8 steps from the position of the rotor as shown in Fig. 3.6. The two stable positions are thus 16 steps apart.

If the rotor aligned at the stable position eight steps to the left (in Fig. 3.6) and movement to the left is towards track 000, the retract micro-switch would be opened, when this occurs, the logic feeds 125 Hz clock pulses to the up/down counter until the positioner has reversed back and opened the micro-switch again. Clearly, since the initial condition of the counter is 1000, its final condition when eight clock pulses have been fed into the counter and the positioner has reversed the eight steps back to the micro-switch again will be 0000. In other words, the rotor S pole in Fig. 3.6 would have initially moved to a position midway between the four stator N poles to the left. And the logic alters the up/down counter condition until these four norths have been shifted to the right by eight steps and replaced the four stator S polarities.
By inspection of Fig. 3.6 this stator condition corresponds to line 1 when the up/down counter condition is 0000. The positioner is thus stationed at an exact multiple of 16 steps from track 000 with the up/down counter condition at 0000.

The retract micro-switch is designed to permit the positioning mechanism to retract a further 8 steps after having opened the switch. Thus if the rotor moves to the alternative stable state 8 steps to the right in Fig. 3.6. when the power supplies are re-applied, the positioning mechanism will have moved to the absolute limit of the retracted position.

If the start button is pressed, the logic feeds 125 Hz pulses into the up/down counter causing the positioning mechanism to be driven forward. When eight variable clock pulses have been fed into the counter, the retracted micro-switch is just on the point of being closed. At the same instant the condition of the counter is again 0000. This condition is repeated every 16 steps of the forward stroke until it reaches track 000. The positioning mechanism has to move a total of 400 steps before it is stopped at track 000. It has to move forward by 200 steps during the cleaning cycle, reverse and move the 200 steps back to track 000 again.

Thus since 400 steps is a multiple of 16 (25 x 16), the up/down counter cycles 25 times until once again the positioning mechanism reaches track 000. Its condition on reaching this point is clearly 0000. The X1210 informs the control unit that the read-write heads are aligned over track 000. This information serves as a reference for the control unit. Hereon, all seek missions initiated by the control unit up-dates the information within the control unit relating over which track the positioning mechanism is stationed.

The assumption made in this discussion that the retracted micro-switch is an exact multiple of 16 steps away from track 000 is untrue (probably). Nor is it necessary to be an exact multiple of 16 steps away from track 000. It could be 12 multiples of 16 steps plus 3 steps distant. It is of no consequence.

If for example the distance was 12 multiples of 16 steps plus 3 steps (a total of 195 steps), then 3 steps away from the retracted switch the condition of the up/down counter would be 0000. Three steps later, the retract micro-switch would be opened and the condition of the counter would be 1101.

If the supplies are removed and then re-applied and the new condition of the counter were say 1001 (4 steps distant from 1101), the rotor would shift by four steps, retracting the positioner (within the 8 steps tolerance of the micro-switch) by four steps. If the start button is now pressed, the positioner would have to move forward four steps before the micro-switch was closed. Its condition at that instant would be 1101. Three steps from the micro-switch toward track 000, the condition of the counter would be 0000 again. And after moving the 12 multiples of 16 steps would arrive at track 000 with the condition of the counter being 0000.

THE DETENT MECHANISM

When the positioning mechanism reaches its required track destination, it is locked into position and held steady by a detent mechanism. This maintains the read-write heads free from mechanical oscillation thus ensuring the integrity of the data whilst performing read, write or eraze instructions.

The detent mechanism forms an integral part of the positioning mechanism. It comprises a rack which is attached to the side of the positioning mechanism and two electro-magnetically controlled detent pawls.

These pawls are pivot mounted along side of the positioning mechanism with the centres of the pivots parallel to its line of travel. Whilst the positioner is in motion, an electro-magnet associated with each pawl maintains the pawls clear of the rack. To lock the positioning mechanism steady one of the magnets is de-energised releasing its associated pawl to engage with the rack. The positioning mechanism is so set up, that whenever the heads are aligned over an even track, the pawl nearest the cartridge engages with the rack. This pawl is refered to as the even pawl. Conversely, whenever the heads are aligned over an odd numbered track (001, 003 etc.), the pawl farthest from the cartridge engages with the rack. This pawl will be refered to as the odd pawl.

The rack teeth are precision machined to a pitch of twice the track-to-track distance. Alternatively, the pitch may be considered to be equivalent to two steps.

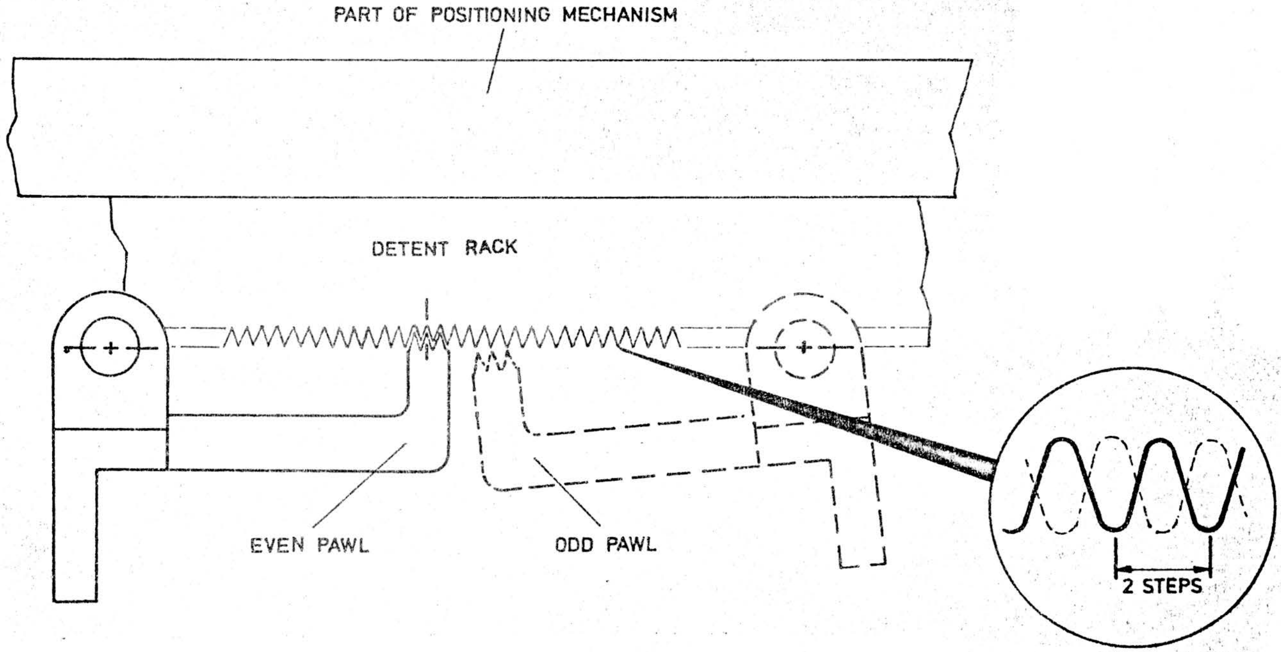


Fig. 3.7 - Detent Mechanism.

Consider in the above diagram that the positioning mechanism is stationary at track 000.

The even pawl electro-magnet would thus be de-energised and the even pawl engaged with the rack. Now consider that this pawl is retracted and the positioning mechanism moved forward by one step to track 001. Since the rack pitch is two steps wide the rack would move to the position shown dotted. The odd pawl magnet would then be de-energised and would engage with the rack. The fine adjustments required to achieve this setting is effected by movement of the pawl pivot points along the axis indicated. This adjustment however is not undertaken in the field.

The Pawl / Logic Relationship.

The detent pawls are controlled by three signals. They are SMCA, DTCZO and $\overline{\text{DETF}}$.

SMCA monitors the logical state of the up/down counters first column. Whenever the positioning mechanism is stationed over an even track, SMCA is at logic 0. Conversely, whenever it is over an odd track SMCA is logic 1. This is utilized by the detent logic to define whether either the odd or the even pawl should be released onto the rack.

The signals DTCZO and $\overline{\text{DETF}}$ are used by the detent logic to define whether either one or both pawls should be retracted from the rack.

A detailed discussion of the detent logic operation is given in the relevant part of the off-line section of this book.

The following table however summarises the relationship between the state of the logic and the pawl positions.

	PAWL CONTROL SIGNALS	PAWL RETRACTED		
		ODD	EVEN	BOTH
LOGIC	SMCA	1	0	-
STATES	DTCZO	0	0	either one or both must be logic 1
	$\overline{\text{DETF}}$	0	0	

OFF-LINE OPERATION

Turn-On Clear. (Fig. 3.9 and 3.10)

When the power supplies are applied to the X1210 a 'turn on clear' circuit on the start/stop/safety logic of card 9 ensures that all X1210 circuits reach their required initial dc conditions before permitting the X1210 to be started. This circuit consists of an RC time delay network; R1 and C1 connected to a transistor switch TS1. The time constant of this circuit is the longest in the electronics unit and is equal to 214 ms. At the instant the dc supplies are connected to the X1210, C1 is in the fully discharged state. Whilst C1 is charging up, its potential maintains TS1 off. Thus the turn on clear signal (TØC) is held at logic 1 for 214 mS after energising the X1210. TØC is inverted and TØC (= 0) causes the signal $\overline{\text{STZFO}}$ to be held 0 until the end of the turn on clear period. $\overline{\text{STZFO}}$ (= 0) sets the Start flip flop to the zero state (STF=0, STF=1), which in turn maintains the Pack motor not Energised signal $\overline{\text{PME}}$ in the 1 state. While this logical condition exists the disk drive motor cannot be started.

The logic circuits are steered to their required initial dc conditions during the 'turn on clear' period by maintaining the master clear signal $\overline{\text{MC}}$ zero throughout the 214 mS. This is effected by the Start-FF signal $\overline{\text{STF}}$ and the signal SSDF. Since $\overline{\text{STF}}$ is in the one state and SSDF is also set to the one state by $\overline{\text{TØC}}$ (=0) then $\overline{\text{MC}}$ is set to 0.

The dominant zero on the master clear line during the 'turn on clear' period sets the following flip flops to the condition indicated (see fig 3.10):

Flip flop	Card	Condition	
Detent	8	DETF=0,	DETF=1
Seek Complete	8	SKCF=0,	SKCF=1
Clean	9	CLF =0,	CLF =1
Start Sequence Control	9	SSCF=0,	SSCF=1
Unsafe	9	USF =1,	
Direction Loaded	11	DLF =0,	DLF =1
Seek	11	SKF =0.	

At the end of the 'turn on clear' period, TS1 is turned on by the potential aquired by the charging capacitor C1.
T0C is therefore set to 0 setting $\overline{\text{T0C}}$ to the one state. The instant $\overline{\text{T0C}}$ becomes 1 all the inputs to the nand gate producing signal SSDF are 'ones'. SSDF is thus set to 0 which in turn sets the master clear signal $\overline{\text{MC}}$ to 1.

Start/Safety Logic (Fig. 3.11)

To ensure that the X1210 cannot be started when no cartridge has been fitted or when the cartridge loading sequence has been incorrectly implemented, three micro-switches, one on the cartridge holder locking ring, another on the rear of the X1210 and the other checking that the cartridge is fully seated in its holder are all connected in series to effectively form an 'and gate. The safety logic on card 9 checks that these three switches are all closed before permitting the X1210 to be started.

When one or more of these-switches are open the not ready to operate signal $\overline{\text{RT0 *}}$ is set to logic 1, $\overline{\text{RT0 *}}$ is inverted and the signal RT0 (= 0) causes the signal $\overline{\text{STFZO}}$ on the reset input of the start-FF to be held at 0. This maintains the Start-FF in the zero state (STF=0, $\overline{\text{STF}}$=1) which in turn holds the signal $\overline{\text{PMEP}}$ at logic 1. And $\overline{\text{PMEP}}$ (=1) together with $\overline{\text{H0D}}$ (=1) sets $\overline{\text{PME}}$ to logic 1. All the time the reset input of the Start-FF is held at logic 0, the logic state on its trigger input is ineffective, regardless of its level. Thus since the trigger input is controlled by the start/stop circuit, the start circuit is effectively inhibited while $\overline{\text{STFZO}}$ is a zero.

If the cartridge is correctly loaded and the X1210 is pushed fully into the rack unit all the micro-switches will be closed and signal $\overline{\text{RT0 *}}$ is set to logic 0. $\overline{\text{RT0 *}}$ is inverted to set RT0 to 1 which together with the signal $\overline{\text{T0C}}$ (=1) sets STFZO to the zero state. $\overline{\text{STFZO}}$ thus becomes logic 1 at hte Start-FF reset input removing the inhibit from the start circuit.

Starting the X1210 (Fig. 3.11)

When the start/stop button is pressed signals $\overline{\text{SSU *}}$ and $\overline{\text{SSD *}}$ are inverted for the duration of pressing the button. $\overline{\text{SSU *}}$ momentarily becomes logic 1 and $\overline{\text{SSD *}}$ logic 0. These signals in turn momentarily change the state of $\overline{\text{SSDF}}$ and SSDF, $\overline{\text{SSDF}}$ going to 0 and SSDF to 1.

$\overline{\text{SSDF}}$ is applied to the Start-FF trigger input setting the flip flop to the one state on the positive going edge of the negative pulse. The start-FF is thus set to STF=1, $\overline{\text{STF}}$=0

If the positioning mechanism is fully retracted, the opened retract position, micro-switch maintains the signal R * at logic 1.
R * is inverted and $\overline{\text{R}}$ (= 0) holds PMSP at logic 1. PMSP (= 1) together with STF (= 1) sets the signal PME to 0. $\overline{\text{PME}}$ is fed to the relay driver on card 3 causing transistors TS7 and TS8 to be turned on, and its output $\overline{\text{PMRA}}$ * to go to zero. A circuit is thus completed from the + 24V dc supply through the switching unit relay and TS8 to the OV line. When the contacts of this relay close, a 220V single phase ac supply is connected to the disk drive motor, running the motor up to speed.

Also at the same instant the start/stop button is pressed, the master clear line is set to logic 0. This ensures as a double-check that the logical states of all circuits set during the 'turn on clear' period is correct. When SSDF is held at logic 1 (for the duration of pressing the start button) it combines with $\overline{\text{STF}}$ (= 1) to set $\overline{\text{MC}}$ to logic 0. At the instant the start button is released, SSDF returns back to the logic 0 condition, $\overline{\text{SSDF}}$ resets the Start-FF, setting $\overline{\text{STF}}$ to logic 0, and the master clear line is returned to logic 1.

Speed OK (Fig. 3.42)

As the disk drive motor accelerates, its speed is optically monitored by the Index and Sector Unit. 16 sector slots and an index slot in the index and sector ring (coupled to the magnetic disk) are sensed by this unit which generates a pulse for each slot sensed. The output of this unit is thus a series of 17 pulses per revolution, of the magnetic disk; 16 of the pulses being sector pulses and one being the index pulse.

The output of the Index and Sector unit is fed to the Speed OK circuit on card 9. This circuit measures the speed of the magnetic disk by measuring the separation between consecutive index pulses. When the magnetic disk reaches full speed, the circuit sets the speed OK signal SPKF to logic 1.

THE CLEANING CYCLE

Initiating the Cleaning Cycle (Fig. 3.12)

When the disk drive motor reaches full speed, the speed OK signal SPKF goes to logic 1 causing the cleaning signal $\overline{\text{CLCY}}$ to be set to 0. At this instant the cleaning cycle commences.

$\overline{\text{CLCY}}$ is set to zero by CLF, $\overline{\text{H0D}}$ and SPKF all being in the 1 state. $\overline{\text{H0D}}$ is held in the 1 state indirectly by CLF being 1. CLF is inverted setting CLFZA to 0 which in turn sets $\overline{\text{HVE}}$ to 1. $\overline{\text{HVE}}$ (=1) is applied to the head valve driver and level shifter circuit on card 3, maintaining its input transistor TS9 in the off condition. This results in TS10 being held off. The output transistor TS11 however is held in the on state setting the head on disk signal H0D to 0- Thus $\overline{\text{H0D}}$ is set to logic 1.

The instant $\overline{\text{CLCY}}$ becomes 0, three significant changes occur in the state of the logic. These are

(a) The Seek complete-FF is reset.
Its output signal $\overline{\text{SKCF}}$ is set to 1 removing the inhibit from the stepmotor drive circuits.

(b) The Detent-FF is reset causing both detent pawls to be lifted from the rack - thus freeing the positioning mechanism.

(c) The inhibit is removed from the gating circuits at the input to the binary up/down counter, enabling the 125 Hz clock to be fed through the trigger input (CP) of the counter.

Enabling the Step Motor Drive Circuits. (Fig. 3.13)

$\overline{\text{CLCY}}$ (=0) causes $\overline{\text{DTCZO}}$ to be set to 0. This signal resets both the Seek Complete-FF and the Detent-FF to the zero state.

The Seek Complete-FF output $\overline{\text{SKCF}}$ becomes logic 1. This signal is applied to all the output gates of the step motor drive circuit. When $\overline{\text{SKCF}}$ is 0, all the gate outputs are set to 1 irrespective of the logical conditions applied to them from the encoding logic. Under these conditions the step motor control windings are all de-energised, a complete inhibit on the control of the motor existing.

The instant $\overline{\text{SKCF}}$ becomes a 1, the output gates of the step motor drive circuit are no longer under the influence of the dominant zero from $\overline{\text{SKCP}}$ the motor aligning itself with the state of the decoding logic.

Lifting Both Detent Pawls (Fig. 3.13)

$\overline{\text{DTCZO}}$ (=0) resets the Detent flip-flop outputs to DETF =0, $\overline{\text{DETF}}$ =1. The signals $\overline{\text{DETF}}$ and DTCZO at the input to the detent nor logic are thus both in the 1 state, setting DETP to logic 0. DETP (=0) sets $\overline{\text{DETP}}$ to 1. Thus irrespective of the state of binary up/down counter output SMCA, both DETDIE and DET2E become 0. These signals control the state of the detent pawl electro-magnets. And when they are 0 their associated electro-magnets are energised lifting the detent pawls clear of the rack.

Both pawl magnet driver circuits are identical, so only the operation of one of them is described.

When $\overline{\text{DET1E}}$ becomes a 0, it forward biases the base-emitter diode of transistor TS9 in its associated detent driver circuit. TS9 is therefore turned on causing the dc level at the base of TS10 to rise. TS10 is bottomed, so providing a circuit from the + 24 v dc supply via R25 the pawl magnet coil and TS10 to the OV line. The electro-magnet is thus energised and the pawl retracted from the rack.

Moving into the Cartridge (Fig. 3.15)

Simultaneous with enabling the step motor drive circuits and lifting both detent pawls, CLCY (=0) enables the 125 Hz clock on card 9 to be fed through to the input of the binary up/down counter.

The 125 Hz clock (3CP) is fed to the input of the binary up/down counter via two gates - one gate is controlled by REL3CP and the other by 3CPP. When both these signals are set to 1 by $\overline{\text{CLCY}}$ becoming 0, the 125 Hz passes through both gates to the counter input.

When $\overline{\text{CLCY}}$ is set to 0, REL3CP is set to 1. This signal is inverted and $\overline{\text{REL3CP}}$ (=0) sets the signal 3CPP to 1. Thus the inhibit is removed from both clock gates and the 125 Hz clock is fed into the counter. This initiates operation of the encoding logic causing the stepping motor to rotate and move the posisioner foreward into the cartridge.

The direction of motion is defined by the logical condition at the U/$\overline{\mathrm{D}}$ input to the up/down counter. When U/$\overline{\mathrm{D}}$ is set to a one (as in this case), the cyclic rotation of the counter outputs Q1 to Q 4 is from 0000 to 1111. Each time 1111 is reached the counter resets to 0000 and commences counting through to 1111 again. This process continues ad infinitum whilst clock pulses are being fed into counter, the cyclic rotation driving the positioner forward at a rate of 125 steps/sec.

The logical condition at U/$\overline{\mathrm{D}}$; $\overline{\mathrm{SMCUP}}$ =1, is defined by the Return to Zero-FF signal $\overline{\mathrm{RTZF}}$ and signals $\overline{\mathrm{RTRP}}$ and $\overline{\mathrm{SKFWD}}$. These three signals are all in the 1 state.

$\overline{\mathrm{RTZF}}$ is set to 1 by the retract position micro-switch. Since the positioner is fully retracted (before and at the instant $\overline{\mathrm{CLCY}}$ goes to 0) its output signal R * is at logic 1. R * is inverted and $\overline{\mathrm{R}}$ (=0) sets $\overline{\mathrm{SKINH}}$ to 0. $\overline{\mathrm{SKINH}}$ (=0) is applied to the Return to Zero-FF setting its output $\overline{\mathrm{RTZF}}$ to 1

$\overline{\mathrm{RTRP}}$ is set to 1 by the speed=0 signal SPZ. Shortly after the disk drive motor has been started SPZ is set to 0 setting PMSP to 1. PMSP (=1) and STF (=1) together set $\overline{\mathrm{PMEP}}$ to the zero state which in turn sets $\overline{\mathrm{RTRP}}$ to 1.

SKFWD is set to logic 1 by the Clean-FF signal CLF (see fig 3.15) CLF, set to 1 by the master clear pulse, is inverted to set $\overline{\mathrm{CLFZA}}$ to 0. This sets $\overline{\mathrm{HVE}}$ to 1 and thus HVE to 0. HVE (=0) causes the seek inhibit signal $\overline{\mathrm{SKINH}}$ to be set to 0 which in turn sets SKFWD to 1.

When the positioner moves foreward from the fully retracted position, the retract micro-switch closes setting R* to 0 and $\overline{\mathrm{R}}$ to 1. $\overline{\mathrm{RTRP}}$ is maintained in the 1 state under these conditions by the speed=0 signal SPZ, which is in the zero state.

Thus the positioner moves foreward into the cantridge at a rate of 125 steps/sec. The logical conditions of the circuits remaining unchanged throughout the foreward stroke until the innermost track of the magnetic disk is reached.

During this foreward stroke the signal HVA * is maintained at logic 1 by the condition of the Clean-FF signal CLF (=0). The solenoid in the head valve is therefore in the de-energised state throughout the foreward stroke. This maintains the head valve shut and prevents the pressurized air supply being applied to the head assembly pneumatic actuators.

Thus during the foreward stroke of the positioner, the nylon cleaning brushes are held down on to the magnetic disk whilst the read-write heads remain retracted within the head assemblies.

Completion of the Cleaning Cycle

When the read-write heads reach track 204 the logic instructs the positioning mechanism to reverse and to simultaneously energise the head valve. The pneumatic supply is fed through the head valve to the head assemblies and pressurizes the pneumatic actuators causing them to load the heads into the flying position and to lift the nylon cleaning brushes from the disk - so ending the cleaning cycle.

Positioning Mechanism Reversal at Track 204 (Fig. 3.16)

The instant of reversal of the positioning mechanism is defined by two variables. These are the state of the track 200 micro-switch and the logical state of the encoding logic signal $\overline{IS12}$. When the track 200 micro-switch is opened by the positioning mechanism and, (shortly afterwards) $\overline{IS12}$ becomes a 0, the $U/\overline{D}$ input of the binary up/down counter is changed from a 1 to 0. This reverses the cyclic rotation of the counter outputs and of the encoding logic, and thus also of the stepping motor. The 125 Hz clock continues however, thus moving the positioning mechanism back towards track 000 at 125 steps/sec.

When the track 200 micro-switch is opened by the positioner, $\overline{H0200}$ is set to 1 setting $\overline{H0200}$ to a 0. After the positioner has moved foreward by (say) 3 more steps (subjest to variation by adjustment) the signal $\overline{IS12}$ also becomes a 0. Both $\overline{H0200}$ and $\overline{IS12}$ are applied to a nor gate. And since they are both 0 the gate output signal T204 becomes 1.

T204 (=1) is applied together with the Start Sequence Control-FF signal SCSF (=1) to a nand gate setting the output of the gate to a 0. This 0 is applied to the Return to Zero-FF, resetting the flip-flop to the 1 state (RTZF=1, RTZF=0).

RTZF (=1) is inverted setting $\overline{RTZFZA}$ to 0 which in turn resets the Clean-FF to the zero state (CLF=0, CLF=1). When the Clean-FF is reset it simultaneously ends the cleaning cycle by setting the Cleaning signal $\overline{CLCY}$ to 1.

$\overline{\text{RTZF}}$ (=0) resets the $\text{U}/\overline{\text{D}}$ input ($\overline{\text{SMCUP}}$) to the binary up/down counter to 0, resulting in reversal of the counter operation - and thus also of the positioning mechanism.

$\overline{\text{RTZF}}$ (=0) also holds both REL3CP and 3CPP in the 1 state when $\overline{\text{CLCY}}$ becomes a 1 at the end of the cleaning cycle. This maintains the 125 Hz gates at the input to the up/down counter enabled during the reverse stroke of the positioning mechanism from track 203 to track 000.

Energising the Head Valve (Fig. 3.17)

At the instant of reversal of the positioner, when the Clean-FF is reset and CLF becomes 0, $\overline{\text{CLFZA}}$ becomes 1. $\overline{\text{CLFZA}}$ along with the signals SPKF (=1), STF (=1) and $\overline{\text{HU000}}$ (=1) completes the logical requirements to set the head valve energised signal $\overline{\text{HVE}}$ to 0. $\overline{\text{HVE}}$(=0)is applied to the valve driver and level shifter circuit on card 3 and initiates two functions.

$\overline{\text{HVE}}$ (=0) forward biases the base-emitter diode of transistor TS9, driving TS9 into the conduction region. The resultant voltage developed across R22 in turn forward biases the base-emitter diode of TS10, bottoming the transistor. Thus the head valve activated signal $\overline{\text{HVA}}$ *becomes logic 0. This completes a circuit from the 24V dc supply, through the head valve solenoid and TS10 to the 0V line, energising the solenoid and causing the head valve to open. The pneumatic supply is thus fed through the head valve to the head assemblies.

When TS10 is bottomed, GR1 is forward biased, the potential at the common anode point of GR1 and GR2 falling to approximately IV. Thus the potential at the base of TS11 falls accordingly turning off the transistor. Its collector potentials thus rises to+5V (almost) setting the head on disk signal HØD to logic 1. HØD (=1) is inverted and $\overline{\text{HØDZA}}$ * (=0) is fed from the X1210 to the computer system. This informs the system that the heads have been loaded into the flying position and the cleaning brushes retracted from the disk. It is an essential part of the system security logic that the computer system receives and interprets this signal. If the heads were not loaded into the flying position and this was ignored by the system, valuable write-data sent to the X1210 while on-line would not be recorded on the disk and would thus be permanently lost.

With the cleaning cycle completed and the heads loaded, the positioning mechanism moves towards the outermost track of the disk (track 000) at a velocity of 125 steps/sec..

Shortly after reversal, the track 200 micro-switch is released by the positioner allowing the switch to revert to the closed position setting H0200 to 0. $\overline{\text{H0200}}$ is thus set to 1 which together with $\overline{\text{IS12}}$, which is also in the 1 state, sets T204 to 0. When this occurs the dominant zero is removed from the input of the Return to Zero-FF. The flip-flop retains its state however until track 000 is reached, when the logical conditions of the circuits are altered by the track 000 signal $\overline{\text{T000}}$.

STOPPING AT TRACK 000

Sensing Track 000. (Fig. 3.18)

To sense the position of track 000 a signal from the variable clock decoding logic ($\overline{\text{IS00}}$) is combined with an optically-generated signal OPZ *. This is necessary due to the difficulty of sensing track 000 with only a mechanical sensor. The small track-to-track distances make this impractical. An approach to solving this problem by using only the logical conditions of the variable clock decoding logic is equally impractical due to the cyclic operation of the decoding logic circuits.

The optical signal OPZ * is generated by the index unit. This unit optically monitors a flag tooth attached to the underside of the positioning mechanism. The width of this flag is equivalent to 12 steps of the positioning mechanism. The positioning mechanism is so set up that the leading edge of the flag enters the index unit when the heads are six steps from track 000. Thus the output signal from this unit OPZ* becomes active six steps before track 000 is reached and would remain active for a further six steps if it passed on through track 000.

The positioning mechanism is also set up so that the variable clock decoding logic signal $\overline{\text{IS00}}$ is synchronized to become active at track 000. Due to the cyclic operation of the decoding logic, it also becomes active at every 16 steps of the variable clock. Thus $\overline{\text{IS00}}$ =0 at track 000, 016, 032, 048 etc. However, both OPZ*, and $\overline{\text{IS00}}$ must be active simultaneously for recognition of track 000 to occur.

When the heads are six steps from track 000 OPZ* becomes 1 and remains in the 1 state while the flag is within ± 6 steps of track 000. OPZ* is inverted setting $\overline{\text{OPZ}}$ to 0. $\overline{\text{OPZ}}$ is applied together with $\overline{\text{IS00}}$ to a nor gate to generate the track 000 signal T000. Thus the instant track 000 is reached and $\overline{\text{IS00}}$ becomes 0, T000 becomes 1 T000 (=1) is inverted and $\overline{\text{T000}}$ (=0) is fed to the Start Sequence Control-FF and the Return to Zero-FF resetting them both to the zero state (RTZF = 0, $\overline{\text{RTZF}}$ = 1: SCSF = 0, $\overline{\text{SCSF}}$ = 1).

Inhibiting the Variable Clock at Track 000 (Fig. 3.18)

The instant the Return to Zero-FF is reset to the zero state, its output signal $\overline{\text{RTZF}}$ (=1) causes the 125 Hz clock gate to be inhibited, so preventing any further 125 Hz clock pulses being fed to the binary up/down counter.

Since both $\overline{\text{CLCY}}$ and $\overline{\text{RTRP}}$ are 1, the instant $\overline{\text{RTZF}}$ becomes 1, REL3CP is set to 0. REL3CP is fed to the 125 Hz clock gate (3CP) setting its output SKCPP permanently to 1. When the clock input to the up/down counter is stopped the outputs from the decoding logic also stop, simultaneously stopping the stepping motor and thus also the positioning mechanism. However, due to the momentum of the moving parts the positioning mechanism overshoots the required position. But since the motor control coils are held energised for the track 000 position a magnetic restoring force is generated by the control windings pulling the rotor back towards track 000. Overshoot again occurs, the rotor and thus also the positioning mechanism performing damped oscillations about the final position (track 000). The worst case condition that this occurs under is at the end of an on-line seek mission whose terminal velocity is 500 steps/sec. This is fully discussed later at the relevant point.

To ensure that these oscillations have completely decayed before releasing a detent pawl onto the rack and locking the positioning mechanism into position, a 24 ms delay circuit is initiated by the reset state of the Return to Zero-FF.

24ms Delay (Fig. 3.19)

The 24ms delay circuit is initiated when REL3CP is set to 0 by the Return to Zero-FF. REL3CP (=0) is inverted setting $\overline{\text{REL3CP}}$ to 1 which together with the Direction Loaded-FF signal $\overline{\text{DLF}}$ (=1) sets the delay time counter reset signal DTCZO to 0.

This sets $\overline{\text{DTCZO}}$ to 1. DTCZO (=1) performs three functions. It sets the reset input of the 24/40 ms delay 4-bit counter to 1. This enables the counter to accept and respond to clock pulses on its C1 input. Also $\overline{\text{DTCZO}}$ (=1) resets the 500Hz divider flip-flop. When input S 2 of this flip-flop is set to 0 its outputs are permanently set to the zero state (2CP = 0, $\overline{\text{2CP}}$ = 1). However, the instant $\overline{\text{DTCZO}}$ becomes 1 the flip-flop commences operating and feeds 250 Hz clock pulses (2CP) to the input of the 4-bit counter.

The four outputs DTCA, DTCB, DTCC and DTCD of this four column counter are illustrated in the waveform diagram of fig3.19. DTCA is half the input frequency and this equal 125 Hz. DTCB is one quarter the input frequency whilst DTCC is one eighth the input frequency

The 24 ms delay is effected by applying signals DTCB and DTCC to the input of an nand gate. Thus when both these signals are in the 1 state, the gate output signal, $\overline{\text{DETFZ1}}$ is set to 0. For DTCB and DTCC to both be in the 1 state, six 250 Hz clock pulses must be fed into the counter input. On the negative going edge of the sixth clock pulse DTCB is set to 1. And since DTCC is already 1, $\overline{\text{DETFZ1}}$ is set to 0.

$\overline{\text{DETFZ1}}$ (=0) is applied to the detent nor logic, causing the appropriate pawl to be released onto the detent rack. Thus the total time taken between recognition of track 000 (resetting the return to zero-FF) and releasing the detent pawl is equivalent to six 250 Hz pulses. This period is 24 ms.

Releasing a Detent Pawl onto the Rack (Fig. 3.19)

The third function performed by $\overline{\text{DTCZO}}$ when it is set to 1 is to remove the dominant 0 from the input of the Detent-FF. Thus when $\overline{\text{DETFZ1}}$ becomes 0 at the end of the 24 ms delay period, it resets the Detent-FF to DETF = 1, $\overline{\text{DETF}}$ =0. Both signals DTCZO and $\overline{\text{DETF}}$ at the input to the detent pawls logic are therefore in the 0 state, causing $\overline{\text{DETP}}$ to be set to 0.

Since the positioner is set up so that the outputs on Q1,Q2,Q3 and Q4 of the binary up/down counter are all 0 when the positioner is at track 000, the signal SMCA (on Q1) is 0.

SMCA and $\overline{\text{DETP}}$ both in the 0 state sets signal $\overline{\text{DETDIE}}$ to 1. This signal is applied to the detent driver circuit on card 2, causing its input transistor TS9 to be turned off. As a result, the junction of resistors R23 and R24 falls almost to 0V, reverse biasing the base-emitter diode of transistor TS10 and turning it off. The collector of transistor TS10 rises to almost 24V, de-energising the even detent pawl electro-magnet and causing the even pawl to be released onto the detent rack.

16 ms Delay (Fig. 3.19)

To allow for the time required for the pawl to move from the fully retracted position to the detent rack. And also to ensure that the natural frequency of oscillation of the carriage due to the pawl striking the rack has fully decayed before initiating a read, write or eraze instruction (when on-line), a further 16 ms delay is effected before inhibiting the step motor and informing the computer system that the heads are at the required track position.

The further 16 ms delay is effected by applying outputs DTCB and DTCD of the 4-bit counter to a nand gate. Thus when both these signals are in the 1 state, the gate output, $\overline{\text{SKCFZ1}}$ is set to 0. For both these signals to be 1 simultaneously, ten 250 Hz clock pulses must be fed into the counter input. Thus on the negative going edge of the tenth input clock pulse; four pulses after resetting the Detent-FF, $\overline{\text{SKCFZ1}}$ becomes 0 and resets the Seek Complete-FF to the 1 state (SKCF =1, $\overline{\text{SKCF}}$ =0).

The reset outputs of the seek complete-FF performs two functions.

$\overline{\text{SKCF}}$ (=0) is applied to each output gate of the step motor decoding logic setting the outputs to 1. This causes all the step motor coil drive amplifiers to be switched off ($\overline{\text{CD1E}}$ = $\overline{\text{CD2E}}$ = $\overline{\text{CD3E}}$ = ... $\overline{\text{CD8E}}$ = 24V).

SKCF (=1) is fed to a gate on card 9 together with signals HVE (=1) and $\overline{\text{T204}}$ (=1) causing the head on track signal (HØT) to be set to 1. HØT (=1) is fed to the X1210 output circuits on card 12 and inverted setting $\overline{\text{HØTZB*}}$ to 0. Thus 40 ms after sensing track 000, $\overline{\text{HØTZB*}}$ (=0) is fed out of the X1210 to the control unit, informing the computer system that the X1210 is ready for on-line operation.

X1210 CONTROL SIGNALS

Input Signals

Control of the X1210 is effected by eight parallel instrucion lines (bit 0 to bit 7) together with one of three tag signals. An instruction from the computer system is only accepted by the X1210 while one of these tag signals is active. Moreover, the instructions implemented depend upon which tag signal is present. Thus when the difference select tag signal (tag 1) is active, difference select instructions (in bcd form) are fed via the relevant instruction lines into the X1210. Similarly, when the head select or control select tag signals (tag 2 and tag 3) are active, head selection or control selection instructions are fed into the X1210 logic circuits and implemented accordingly.

Difference Select Instructions

The difference select instructions inform the X1210 of the difference between the actual track position and the required track position. These instructions are supplied via the bit 0 to bit 7 bus-lines when the tag 1 signal is active.

Head Select Instruction

The head select instruction informs the X1210 which head should be selected. The instruction is supplied via the bit 0 bus-line when the tag 2 signal is active. If bit 0 is active, the upper head is selected. Conversely if bit 0 is inactive, the lower head is selected.

Control Select Instructions

The control select instructions comprise six separate commands which are supplied via the respective bus-lines indicated below when the tag 3 signal is active. Note however that all these commands cannot be conveyed simultaneously.

The six commands are:

(a) Write Enable (bus 0): switches on the write drivers.
(b) Read Enable (bus 1): switches on the read amplifier.
(c) Seek Foreward (bus 2): This instructs the positioning mechanism to move towards the centre of the disk.

(d) Eraze Enable (bus 4): Switches on the eraze amplifier

(e) Seek Reverse (bus 5): This instructs the positioning mechanism to move towards the outer track of the disk.

(f) Return to Zero(bus 6): The heads return to track 000

X1210 Output Signals

The X1210 supplies the following status signals to the control unit:

(a) Index Pulse : This is a pulse generated once per revolution of the disk. It serves as a reference point for the sector pulses.

(b) Sector Pulses : These pulses are generated 16 or 24 times per revolution of the disk - dependant on the type of cartridge used. In conjunction with the index pulse these pulses define the precise sector of the track passing between the heads.

(c) Unsafe : This signal informs the control unit that a fault condition due either to a wrong input command or to failure within the X1210 exists.

(d) Head on Disk: This signal informs the control unit that the heads have been loaded into the flying position and the cleaning brushes are retracted from the disk.

(e) Head on Track : This signal informs the control unit that the positioning mechanism has reached the required track position and has been locked into position by the detent mechanism.

Note

It is an inherent part of the control unit logic that it receives the head on disk signal before the head on track signal. This is necessary to ensure the integrity of the write data.

The Input Circuits (Fig. 3.20 and 3.44)

Each input circuit to the X1210 is as shown in Fig.

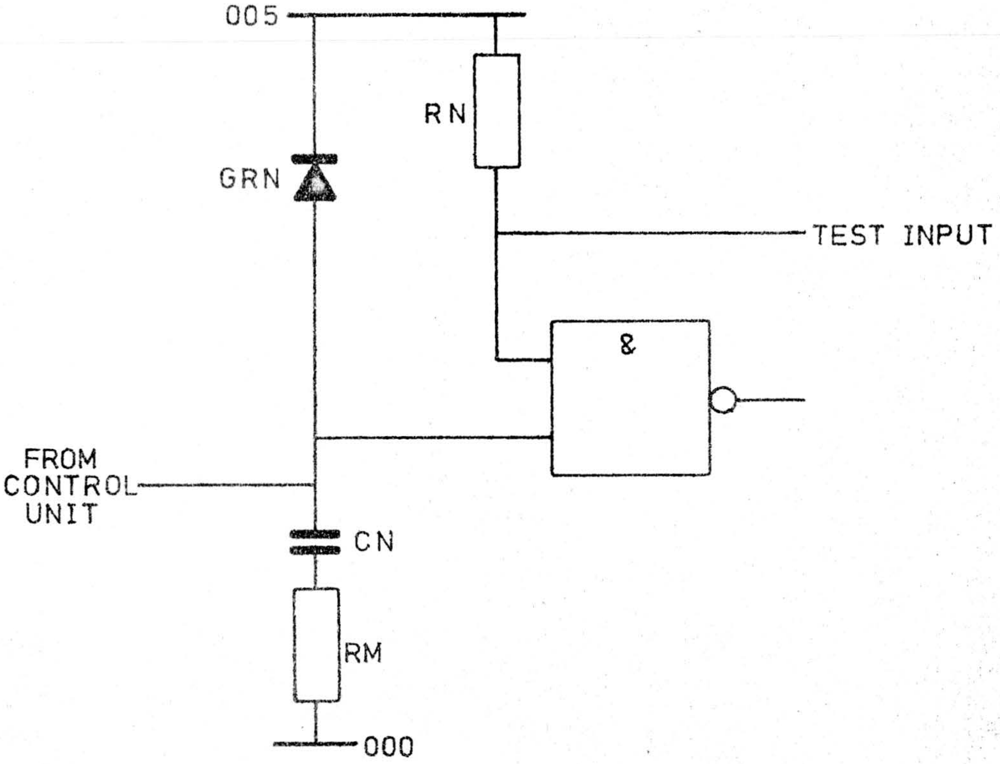


Fig. 3.20 X1210 Input Circuit.

The circuit has two inputs. One input is for test purposes only and is connected to the test module edge connector in the electronics rack. To hold the test input to the nand gate at logic 1, it is permanently connected to the +5V dc line via resistor Rn. The other input is connected by the transmission line to the control unit.

When the control unit output line is inactive, the voltage level at the input to the nand gate is approximately +5V. Thus both inputs to the nand gate are high under these conditions setting the output of the gate to logic 0.
A negative command pulse issued by the control unit momentarily sets the input of the gate to almost ov. This sets the gate output to logic 1 for the duration of the pulse. This logical state is interpreted by the X1210 as either difference select, control select or head select instructions accordingly - dependant on which channel is activated.

The diode G_{RN} serves to clamp the overshoot on the positive going edge of the input pulse. If the overshoot exceeds +5V, the diode is forward biased and conducts limiting the voltage at the gate input to +5·3V. The resistor capacitor combination Rm Cn slows the positive going trailing edge of the input pulse thus also minimising the voltage overshoot amplitude.

The Output Circuits. (Fig. 3.21 and 3.44)

Each output circuit is as shown below.

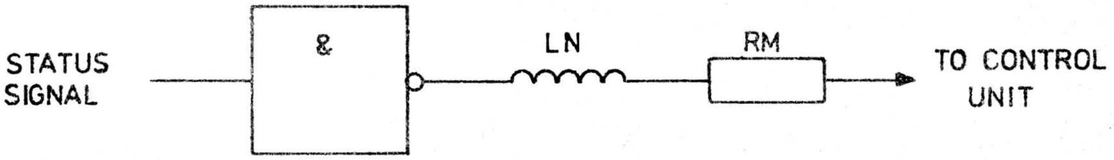


Fig. 3.21 X1210 Output Circuit.

When the status signal is inactive, the dc level at the gate input is approximately 0V. This is inverted setting the gate output to logic 1 (+5V). Damping of high frequency ripples or spikes is effected by the series filter formed of Rm Ln.

Decoding the Difference Select Instructions

The difference select instructions are interpreted by the decremental counter. This counter comprises two four column counters J and Q connected in series as shown in fig. 3.22

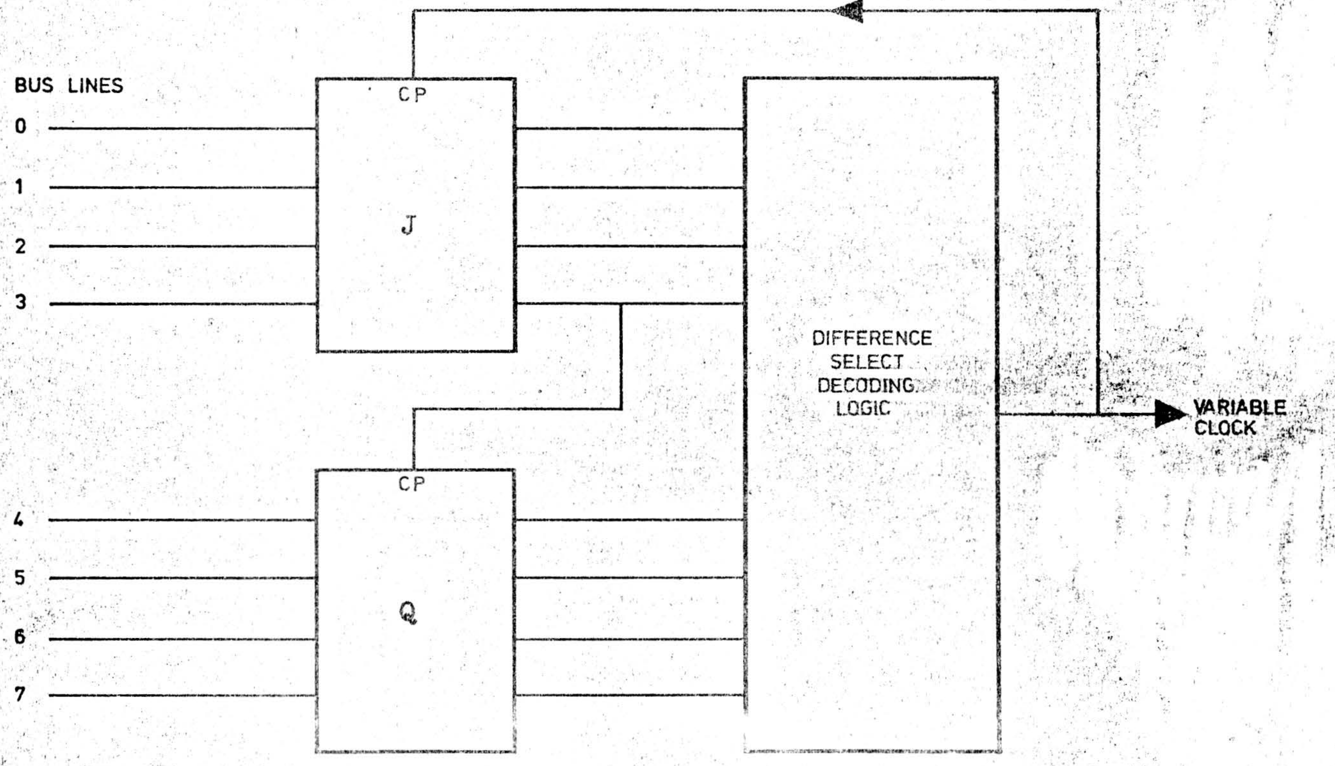


Fig. 3.22 Difference Select Decoding

The contents of the counters J and Q are indicated by the logical state of the eight outputs which are monitored by the decoding logic. When these counters are both full, the state of these outputs are all at logic 1. While this logical condition of "all ones" is sensed by the decoding logic the variable clock gate is inhibited.

The four inputs to J and Q connected to the bus lines serves to pre-fill the counters during the event of the tag 1 pulse. The instant the tag 1 line becomes active (logic 0), the difference select instructions on the bus lines (logic 0) pre-fill the two counters.

When the tag 1 pulse becomes inactive the decoding logic senses that the contents of J and Q are not all at logic 1 and enables the variable clock gate. The variable clock pulses are fed simultaneously to both the stepping motor and to the input of the decremental counter. Each pulse fed to the stepping motor causes the positioning mechanism to be moved radially by one track of the magnetic disk. Meanwhile, each pulse fed to the decremental counter decreases the difference select data stored in counters J and Q by one pulse. Since the number of pulses required to completely fill the counters to a state of "all ones" equals the number of pulses required to move the positioning mechanism by the required number of tracks, the instant a state of "all ones" is reached, the required track position is also reached. At this instant the difference select decoding logic recognises that both J and Q are full and simultaneously inhibits the variable clock gate. Thus no further clock pulses are fed to either the stepping motor or to the counters. The positioning mechanism therefore reaches the required track position - as defined by the difference select data - and then stops.

The decremental counter (J and Q) thus functions as a comparator; it contents dynamically changing throughout a seek mission, defining at all instants how many variable clock pulses must be fed to the stepping motor to reach the required track position.

The relationship between the bus lines made active when the tag 1 signal is active and the size of the seek mission is expressed in the following table:

Bus line	No. of Tracks
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

With respect to the table, a seek mission of say 10 steps would be initiated by activating bus lines 1 and 3 during the tag 1 signal.

Alternatively, for a seek mission of say 171 tracks, bus lines 0, 1, 3, 5 and 7 would have to be activated.

Since counter J is filled every 15 pulses of the variable clock and is cleared to 0 by the 16th pulse, this counter handles difference select instructions associated with seek missions of less than 16 steps (as indicated by the table). The difference select instructions associated with seek missions of greater than 16 steps requires pre-filling both counters J and Q (exept for missions of 16, 32, 64, 128 and their sum combinations).

Clearly then, by monitoring the contents of the greater than 16 steps counter (Q), the difference select decoding logic can differentiate between a seek mission of less than 16 steps and one of greater than 16 steps.

Variable Clock Selection

The variable clock frequency selected by the logic can either be 125 Hz, 500 Hz or 1000 Hz. The frequency selected is dependant upon the size of the seek mission.

For a seek mission of less than 16 steps - when the outputs of counter Q are all high - the decoding logic selects the 125 Hz clock. Thus for seek missions of less than 16 steps, the positioning mechanism is driven at a constant velocity of 125 steps /sec.

Maintaining the velocity of the positioning mechanism constant throughout a long seek mission is time consuming. To minimise this time, long seek missions are divided into three sections. For the first 9 steps, and also for the last 6 steps of the seek the variable clock frequency is 500 Hz. For the intermediate steps the frequency is switched to 1000 Hz.

This motion is illustrated in fig. 3.23.

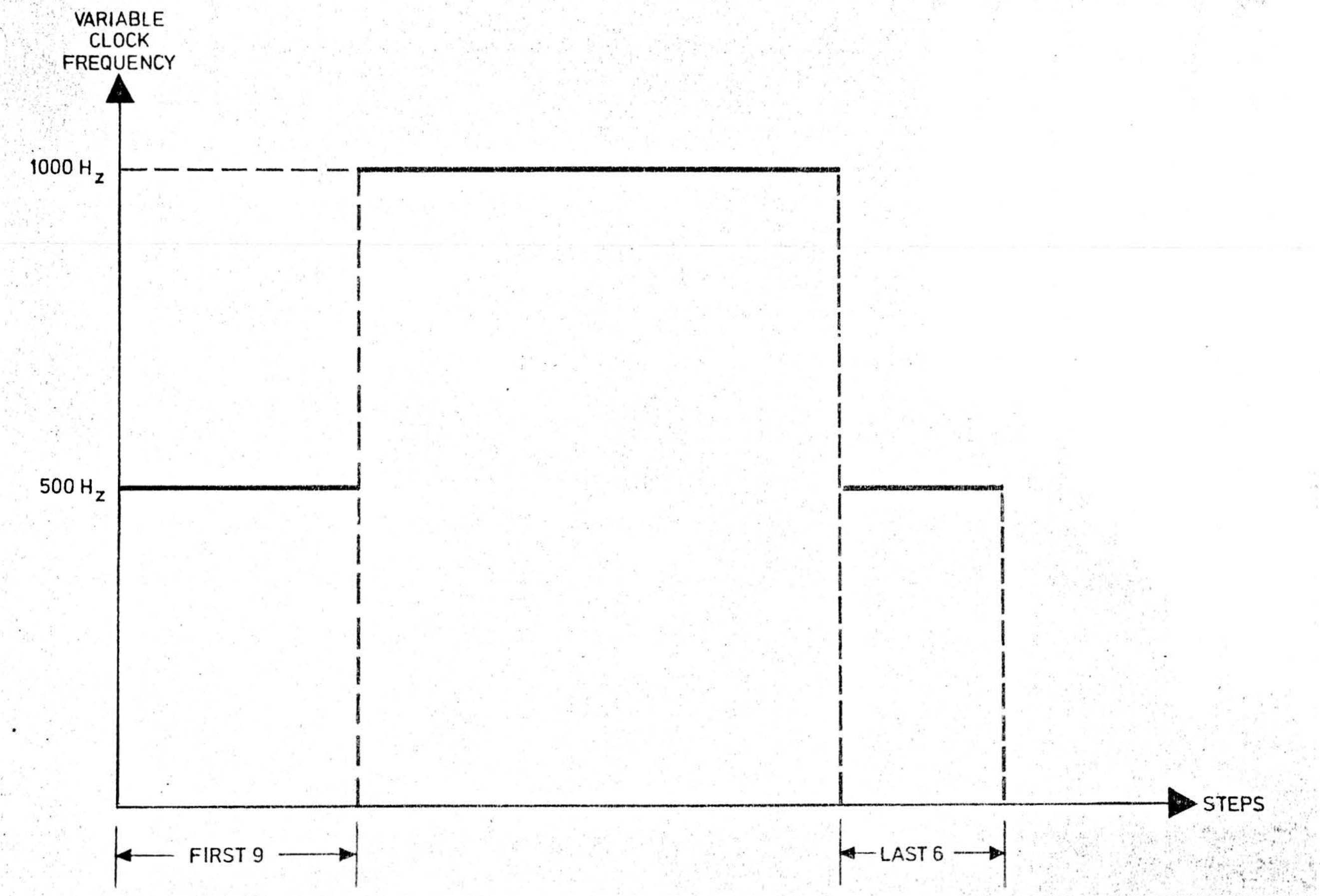


Fig. 3.23 Greater Than 16 Steps Seek Mission.

If for example the positioner had to move by 100 steps. The first 9 steps would be at a velocity of 500 steps/sec. The next 85 steps would be at 1000 steps/sec. And the final six steps would again be at 500 steps/sec.

Dynamics of the Positioning Mechanism

To appreciate the reason for switching the variable clock frequency at the end of the first 9 steps and at the beginning of the last 6 steps, it is necessary to examine the distance-time characteristics of the positioning mechanism.

When a step function is applied to the stepping motor control windings, the rotor initially lags behind the stator magnetic field. This lag is due to friction and the inertia of the rotor and positioner. It causes the control windings to generate a magnetic restoring torque, which in turn causes the rotor to accelerate and overshoot the magnetic field. At the instant of overshoot, the torque on the rotor reverses, causing it to decelerate, overshoot and to lag again.

After a few overshoots have occured, each becoming progressively less than the previous, the rotor finally stabilizes and rotates at the same speed as the magnetic field but with a small steady state error - due to viscous friction. This characteristic is illustrated in fig. 3.24.

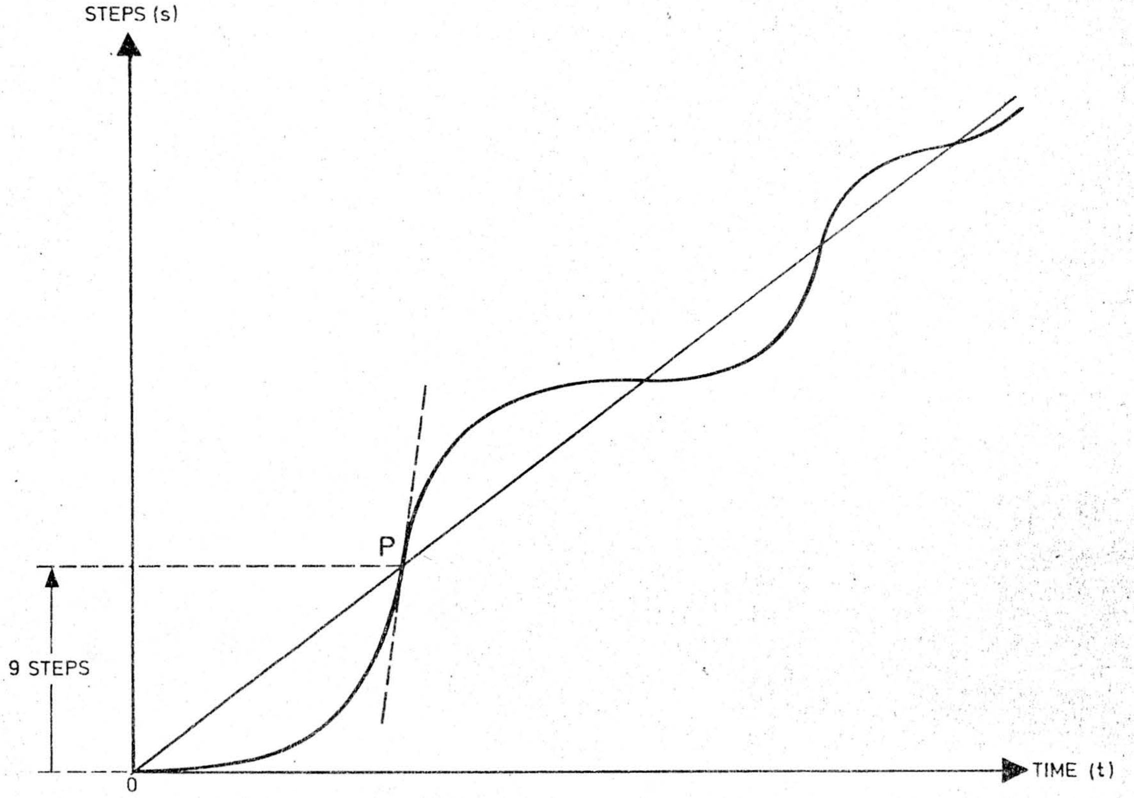


Fig.3.24 Positioner Step Function Response

The important point occuring on this characteristic is at the first overshoot (P). By experiment, it has been found an inherent characteristic of the positioning mechanism that if the stepping motor command signal is at 500 Hz, the velocity momentarily aquired at P ($\frac{ds}{dt}$), is equivalent to the steady - state velocity reached with a command signal of 1000 Hz. The number of steps required to reach this first overshoot P is a constant and is always equal to nine.

This characteristic is utilized by switching the frequency from 500 Hz. to 1000 Hz. when the positioner has moved by 9 steps. Since it momentarily accelerates to 1000 steps/sec. at this instant, the rotor immediately synchronizes with the magnetic field and thereon moves with a constant velocity of 1000 steps/sec.

Two predominant factors affect how the positioning mechanism is brought to rest at the end of a greater than 16 steps seek mission. They are the requirement to maintain the positioner velocity at a maximum (1000 steps/sec.) for as long as possible whilst minimizing its final velocity. This latter requirement is important, since the velocity of the positioning mechanism at the instant the variable clock is stopped determines the damping time required before a read, write or eraze instruction can be implemented.

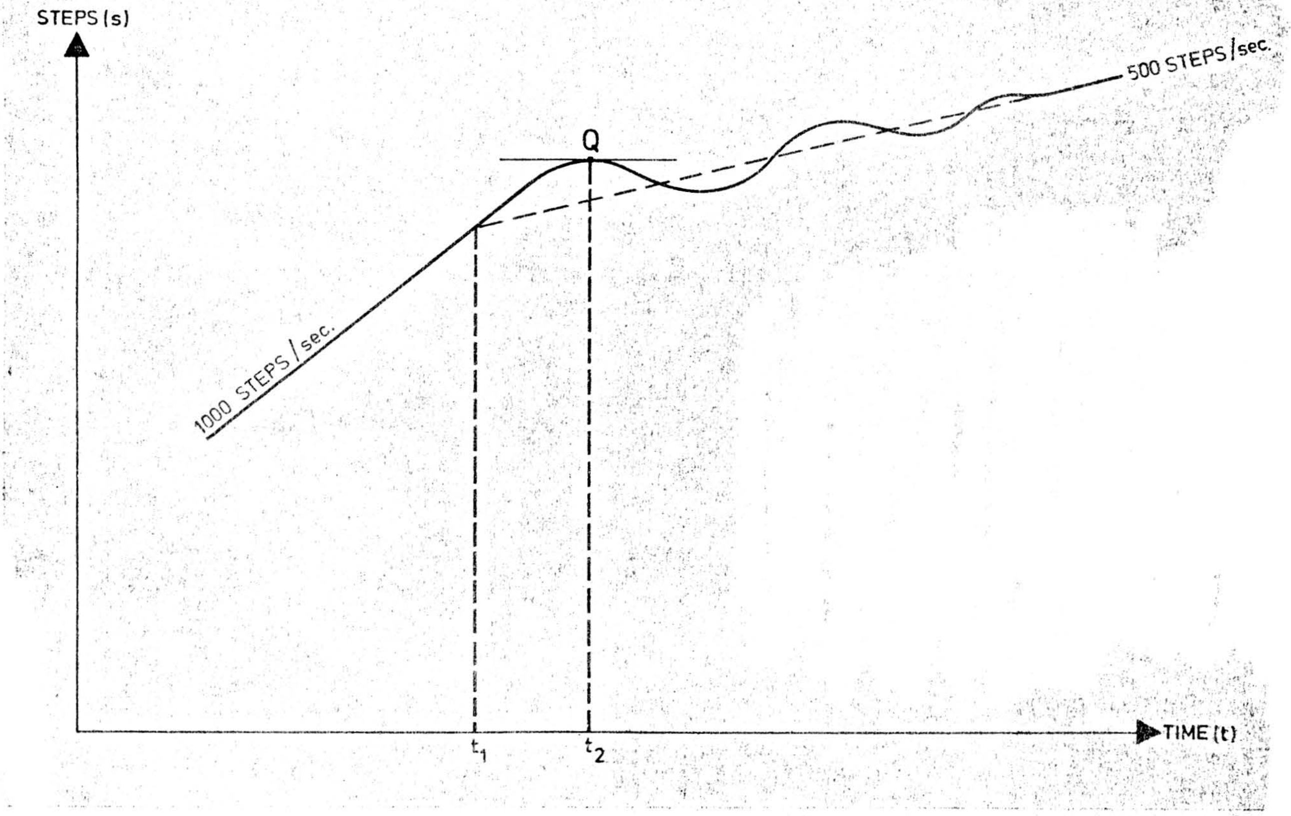


Fig. 3.25 1000/500 Hz Switching Response.

With reference to fig. 3.25. If at t1 the variable clock is switched from 1000 Hz to 500 Hz, then due to the momentum of the moving parts, the positioner initially tends to continue at 1000 steps/sec. Shortly after t1 however it commences to decelerate and would after a number of overshoots finally move at a velocity of 500 steps/sec.

To keep the final velocity of the positioner as low as possible, the variable clock is stopped at the point of minimum velocity on the first overshoot. This point occurs at t2 where the velocity $\frac{ds}{dt}$ at Q is a minimum. It has been found by experiment that point Q always occurs 6 steps after t1. The final velocity at Q is sufficiently low to ensure that the positioner is damped within 24ms of stopping the variable clock - as illustrated in fig. 3.26.

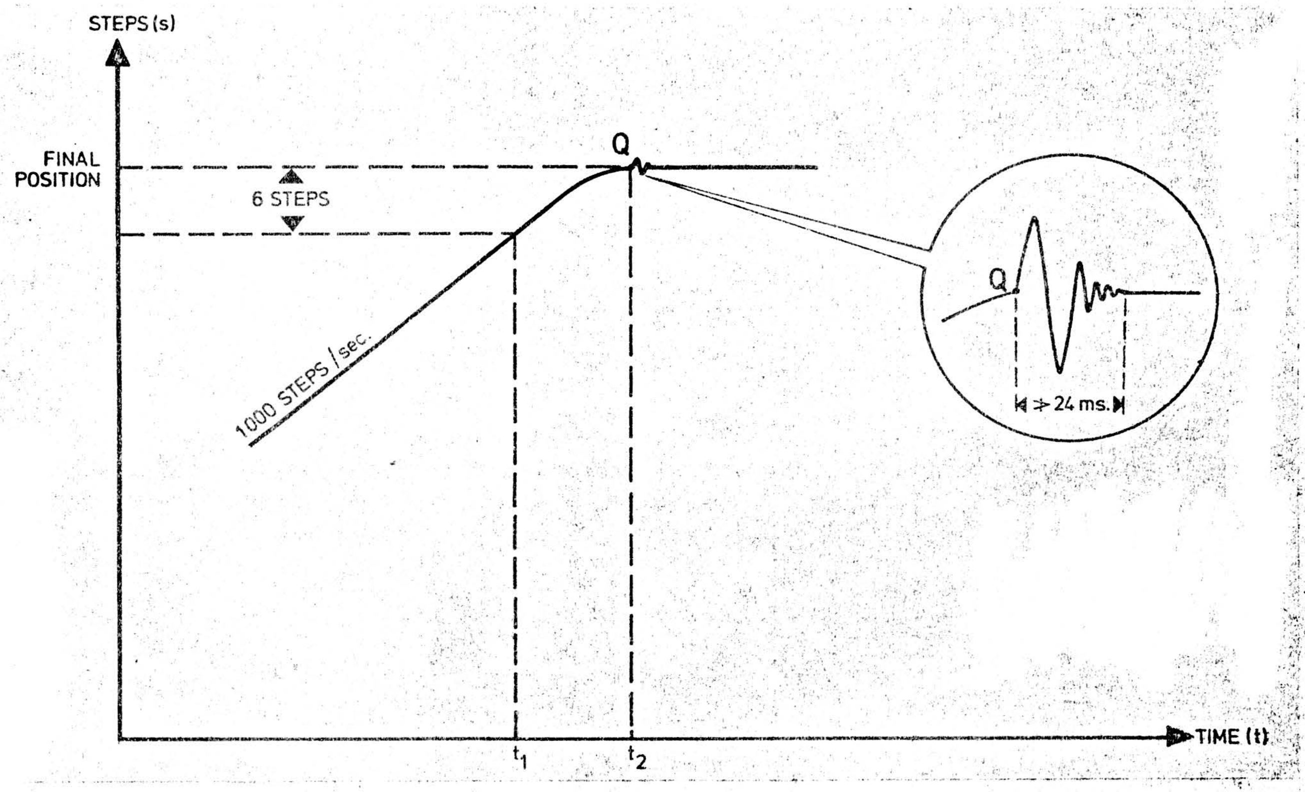


Fig. 3.26 Damping of the Positioner.

A Seek Mission of Greater Than 16 Steps (Fig. 3.29 and 3.30)

A seek mission of greater than 16 steps is best described by considering the operation of a set example. The example described in this book is a seek of 20 steps forward.

Input Signals

A seek mission of 20 steps forward is initiated by:

(a) Activating the $\overline{\text{BUS 2*}}$ and $\overline{\text{Bus 4*}}$ channels simultaneous with the $\overline{\text{TAG 1*}}$ channel. This constitutes the instructions to move by 20 steps.

(b) Activating the $\overline{\text{BUS 2*}}$ and $\overline{\text{TAG 3*}}$ channels (when the $\overline{\text{TAG 1*}}$ channel has been de-activated). This constitutes the instructions to move forward.

When the difference select instructions are fed to the X1210, the $\overline{\text{BUS 2*}}$, and $\overline{\text{BUS 4*}}$ and $\overline{\text{TAG 1*}}$ channels are set to logic 0. These signals are inverted by the transmitter/receiver circuits on card 12, setting the signals BUS 2, BUS 4 and TAG 1 to logic 1. These three signals are in turn inverted setting $\overline{\text{BUS 2 ZA}}$, $\overline{\text{BUS 4 ZA}}$, and $\overline{\text{TAG 1 ZA}}$ at the input to the decremental counter to logic 0.

Pre-filling the Decremental Counter (Fig. 3.29 and 3.30)

The two four-bit counters J and Q forming the decremental counter can each be pre-filled via their input pins D_A, D_B, D_C and D_D, when a negative going edge is present on their strobe inputs. The logical state on pin D_A during the event of the strobe pulse ($\overline{\text{TAG 1 ZA}}$) is transferred to the ones column of the counter. Similarly, D_B pre-fills the two's column whilst D_C and D_D pre-fill the fours and eights columns respectively. Thus for example if one assumes the 1-2-4-8 columns of counter J to be all at logic 1 and the inputs D_A and D_B are set to logic 0, a negative going edge on the strobe input will transfer these zero's to the first and second columns of the Counter. The counter would therefor have been effectively pre-filled with twelve pulses since to reach a state of 1111 again three pulses would have to be fed into the counter trigger input.

Counters J and Q are connected in series to form a 1-255 decremental counter. This is effected by connecting the fourth column of J to the trigger input of Q. Thus for every sixteen pulses fed to J, one carry pulse is fed to Q. After J has counted from 0000 to 1111 sixteen times in succession, sixteen carry pulses would have been generated and fed to Q bringing each of the 1-2-4-8 colums of Q to the 1 state.

The effect of pre-filling both J and Q simultaneously can now be considered. Assuming the initial condition of each counter to be 1111. If D_A on both J and Q are set to 0 while J and Q are strobed, both counters will be set to 1110. This is equivalent to pre-filling the decremental counter with 238 pulse since for J and Q to reach a state of 1111, seventeen pulses must be fed into the trigger input of J.

When-as in this example- the $\overline{\text{BUS 2 ZA}}$ and $\overline{\text{BUS 4 ZA}}$ signals become 0, the fourth column of counter J and the first column of counter Q are set to 0 on the negative going edge of the $\overline{\text{TAG 1 ZA}}$ pulse. This sets J to 1101 and Q to 1110. The decremental counter has effectively been filled with 235 pulses since for both J and Q to reach a state of 1111, twenty pulses must be fed into the trigger input of J.

Recognition of a greater than 16 steps seek (Fig. 3.29 and 3.30)

A seek mission of greater than 16 steps is sensed by monitoring the contents of counter Q on signal lines SCSRE, SCSRF, SCSRG and SCSRH. If the seek is greater than 16 steps, one or more of the 1-2-4-8 columns of Q and thus of these signals become 0 on the negative going edge of the TAG 1 pulse. When this occurs $\overline{\text{L16S}}$ is set to 1 removing the dominant 0 from the "D" input of the Less Than 16 Steps-FF. Since the reset input of this flip-flop is simultaneously set to 1 indirectly by $\overline{\text{L16S}}$ being set to 1, a positive going edge applied to its trigger input will change the state of the flip-flop. Thus since the TAG 1 pulse is connected its trigger input, the Less Than 16 Steps-FF is set to the 1 state (L16F=1, $\overline{\text{L16F}}$=0) on the positive going edge of the TAG 1 pulse. When this occurs a greater than 16 steps mission commences.

The arrangement of the logic monitoring the contents of J and Q is such that irrespective of the size of the seek mission, the effect of pre-filling either J or Q, or both, is to set the reset inputs of the Last 6 Steps-FF, the seek-FF and the Less Than 16 Steps-FF to logic 1. This removes the inhibit from these flip-flops enabling them to be set or reset accordingly.

If for example only columns 2 or 4 of counter J were pre-filled, then either SCSRB or SCSRC would be set to 0. This would cause $\overline{\text{SEX}}$ to become logic 1 and thus $\overline{\text{DLFZO}}$ to be set to 1. And since $\overline{\text{DLFZO}}$ is connected to reset inputs of these three flip-flops, their reset inputs would be held at logic 1.

Alternatively, if only columns 1 or 8 of counter J were pre-filled, SCSRA or SCSRD would be set to 0. This would set L6S to 1. And L6S (=0) would set $\overline{\text{SEX}}$ to 1 giving the same result as before.

The logical state of the Less Than 16 Steps-FF determines which variable clock frequency is fed to the stepping motor. If it is still in the zero state after the event of the TAG 1 pulse, it enables only the 125 Hz clock to be fed to the stepping motor throughout the seek mission.

This only occurs when counter J has been pre-filled - as on a less than 16 steps seek mission. When it is set to the 1 state however, it enables both the 500 Hz and the 1000 Hz clocks to be used during the relevant periods of the seek mission.

Clearly for a seek forward of 20 steps the difference select data will cause the less than 16 steps-FF to be set to the 1 state.

Inhibiting the 125 Hz Clock (Fig. 3.29 and 3.30)

When the less than 16 steps-FF is set to the 1 state, its output $\overline{\text{L16F}}$ (=0) is applied together with the 125 Hz clock to a nand gate setting its output 3CPZA to logic 1.

First 9 Steps Counter Reset (Fig. 3.29 and 3.30)

Before the Less Than 16 Steps-FF is set to the 1 state, its output L16F (=0) maintains the first 9 steps counter in the reset state by setting $\overline{\text{F9SCZO}}$ on its reset input to logic 0. The 1-2-4-8 columns of this 4-bit counter are all held in the zero state under these conditions. Signals F9SCA and F9SCD monitoring the first and eighth columns of the counter are thus both 0 causing $\overline{\text{F9S}}$ to be held at logic 1.

When the Less Than 16 Steps-FF is reset to the 1state, L16F (=1) removes the dominant 0 from the reset input of the counter by setting $\overline{\text{F9SCZO}}$ to logic 1. The state of the counter remains the same however. And thus F9SCA andF9SCD remain logic 0. This condition is maintained until the variable clock gate is opened. When this occurs the variable clock pulses are fed into this counter (and also the decremental counter and the stepping motor). The eighth column of this counter remains 0 until the ninth input clock pulse.

Inhibiting the 1000 Hz Clock (Fig 3.29 and 3.30)

Whilst the first or eighth columns of the first 9 steps counter are at logic 0, F9SCA or F9SCD remains 0. Thus $\overline{\text{F9S}}$ is maintained at logic 1, holding F9S at 0. F9S (=0) is applied together with the 1000 Hz clock (OCP) to a nand gate. The output of this gate (OCPZA) is therefore held in the 1 state.

Enabling the 500 Hz Clock (Fig. 3.29 and 3.30)

When the Less Than 16 Steps-FF is set to the 1 state, its output L16F (=1) is applied together with the 500 Hz clock (1CP) to a nand gate and enables the clock pulses to pass through the gate. The gate output ICPZA is an inversion of 1CP. ICPZA is applied together with 3CPZA and OCPZA to a further nand gate. And since both of the latter signals have been set to the 1 state (by inhibiting the 125 Hz and 1000 Hz clocks) the 500 Hz clock pulses pass through this gate generating 500 Hz on its output SKCP. SKCP is inverted twice to make SKCPZB active at 500 Hz on the trigger input of the Seek-FF and on the input of the variable clock gate. The 500 Hz clock pulses cannot pass through the variable clock gate until the Seek-FF has been set to the 1 state by the control select instructions however.

Instructions to Move Forward (Fig. 3.29 and 3.30)

The instructions to move forward are received by the X1210 when the BUS 2* and TAG 3* channels on the input circuits (card 12) are set to 0. These signals are inverted by the input circuits setting the BUS 2 and TAG 3 lines to 1. These two signals are fed to a nand gate setting its output $\overline{\text{FWDFZ1}}$ to 0. $\overline{\text{FWDFZ1}}$ (=0) is fed to both the Forward-FF and the Direction Loaded-FF. The Forward-FF is set to FWDF=1, $\overline{\text{FWDF}}$=0 whilst the Direction Loaded-FF is set to DLF=1,DLF =0.

$\overline{\text{FWDF}}$ (=0) is fed to card 8 setting SKFWD to logic 1. SKFWD is applied together with $\overline{\text{RTRP}}$ and $\overline{\text{RTZP}}$ to a nand gate whose output, SMCUP defines the logical condition $\overline{\text{SMCUP}}$ on the U/$\overline{\text{D}}$ input of the binary up/down counter. Since both $\overline{\text{RTRP}}$ and $\overline{\text{RTZP}}$ were set to logic 1 at the end of the cleaning cycle at track 000 (see fig. 3.16) all the inputs to the gate defining SMCUP are logic 1. SMCUP is therefore set to 0. This is inverted to set $\overline{\text{SMCUP}}$ on the U/$\overline{\text{D}}$ input of the counter to logic 1. And when U/$\overline{\text{D}}$ is a 1, the cyclic rotation of the up/down counter is in such a direction that the variable clock pulses drive the positioning mechanism forward.

Enabling the Variable Clock Gate (Fig. 3.29 and 3.30)

When the Direction Loaded-FF is reset to the 1 state by the seek forward instructions, its output DLF (=1) removes the dominant 0 from the "D" input of the Seek-FF. Since the reset input of this flip-flop has already been set to 1 by the difference select instructions (DLFZO=1), its state will be altered by the first positive going edge on its trigger input. The 500 Hz clock pulses have been present on the input to the variable clock gate and also on this trigger input since the positive going edge of the TAG 1 pulse. Thus the first positive going edge of the 500 Hz clock on the Seek-FF trigger input occuring after the Direction Loaded-FF is set to the 1 state by the seek forward instructions, resets the Seek-FF to the 1 state (SKF=1).

The Seek-FF output SKF (=1) is fed together with the 500 Hz clock to the nand gate constituting the variable clock gate. And at the instant SKF goes to 1, the 500 Hz pulses pass through the gate on signal line $\overline{\text{SKCPZC}}$ and after inversion on SKCPZC to the decremental counter, the first 9 steps counter and to the binary up/down counter.

The variable clock pulses (500 Hz) have to pass through two nand gates before they can be fed into the trigger input of the up/down counter. The first gate is controlled by the seek inhibit signal $\overline{\text{SKINH}}$ and by signal $\overline{\text{REL3CP}}$. Unless an unsafe condition arises, $\overline{\text{SKINH}}$ remains at logic 1 throughout on-line operation of the X1210. The other signal - $\overline{\text{REL3CP}}$ - is also in the 1 state. It is set to 1 by $\overline{\text{RTZF}}$, $\overline{\text{RTRP}}$ and $\overline{\text{CLCY}}$ all of which are at logic 1. Furthermore they - like $\overline{\text{SKINH}}$ - remain in the 1 state throughout on-line operation. Thus since both $\overline{\text{SKINH}}$ and $\overline{\text{REL3CP}}$ are both 1, the 500 Hz clock pulses pass through the gate on signal line 3CPP to the input of the second nand gate. This gate is controlled by SKCPP. And SKCPP is in turn controlled by REL3CP. Since REL3CP is set to the 0 state by $\overline{\text{RTZF}}$ (=1), $\overline{\text{RTRP}}$ (=1) and $\overline{\text{CLCY}}$ (=1), then SKCPP is set to the 1 state. The 500 Hz clock pulses therefore pass through this second gate on signal line SMCCP to the trigger input of the binary up/down counter. And since the U/$\overline{\text{D}}$ input of the counter has been set to logic 1 by the Forward-FF, the positioning mechanism commences to move foreward. Its velocity is a function of the variable clock frequency (500 Hz) and is 500 steps/sec.

The First 9 Steps (Fig. 3.29 and 3.30)

At the same instant the variable clock gate opens and feeds the 500 Hz clock to the up/down counter, it also feeds the 500 Hz clock to the decremental counter and to the first 9 steps counter.

The 500 Hz has to pass through two gates before it can be applied to the trigger input of the first 9 steps counter. The first gate is controlled by signals $\overline{F9S}$ and $\overline{F9SCZO}$, both of which are at logic 1. $\overline{F9S}$ is held at logic 1 by the outputs F9SCA and F9SCD of the first 9 steps counter which are initially both 0. $\overline{F9SCZO}$ is set to 1 by the state of the Less Than 16 Steps-FF output $\overline{L6SF}$ (=1) and the signal $\overline{REL3CP}$ (=1).

The 500 Hz clock pulses can therefore pass through the first gate and after inversion by the second gate are fed into the first 9 steps counter trigger input on F9SCCP. Since the reset input $\overline{F9SCZO}$ is logic 1, the counter responds to the negative going edge of the 500 Hz clock pulses.

By monitoring the logical condition on the first and eighth columns of the first 9 steps counter with a nand gate, the instant both columns reach the 1 state, the output of this gate, $\overline{F9S}$, is set to logic 0. For the first and eighth column to both reach the 1 state, nine pulses must be fed into the counter. Thus on the ninth 500 Hz clock pulse negative edge, both F9SCA and F9SCD are in the 1 state simultaneously for the first time, setting F9S to 0. This simultaneously stops any further variable clock pulses being fed into the first 9 step counter, since $\overline{F9S}$ (=0) sets the trigger input of the counter F9SCCP to 0.

Changing the Variable Clock from 500 Hz to 1000 Hz (Fig. 3.29 and 3.30)

The instant the first 9 steps counter sets $\overline{F9S}$ to 0, $\overline{F9S}$ prevents any further 500 Hz clock pulses passing through the variable clock gate by setting ICPZA to logic 1.

$\overline{F9S}$ is inverted setting F9S to 1. And since F9S has been inhibiting the 1000 Hz clock (OCP) while in its zero state, the instant it becomes logic 1 it enables the 1000 Hz clock pulses to pass through the gate on signal line OCPZA.

The 1000 Hz clock (OCPZA) is fed together with the signals 3CPZA and ICPZA to the input of a nand gate. Both these latter signals have been set to the 1 state; 3CPZA by the Less Than 16 Steps-FF output $\overline{L16S}$ = 0 and ICPZA by $\overline{F9S}$ (= 0). The 1000 Hz clock is thus fed through this gate making SKCP active at 1000 Hz. After two inversions, the 1000 Hz is applied to the input of the variable clock gate. And since the gate is open, the 1000 Hz is fed on SKCPZC to the trigger input of the binary up/down counter. The 1000 Hz clock takes the same route as the preceeding 500 Hz clock pulses. The positioning mechanism velocity therefore increases accordingly to 1000 steps/sec.

The last 6 Steps (Fig. 3.29 and 3.30)

Meanwhile, the 1000 Hz clock is also fed into the decremental counter. The counter responds to the negative going edges of the variable clock. And when the fifth 1000 Hz clock pulse is fed into the counter, it has been fed with a total of 14 pulses; 9 of them at 500 Hz and 5 of them at 1000 Hz. Thus, since the decremental counter was initially pre-filled with 238 pulses (for a seek of 20 steps), then on the negative going edge of the fifth 1000 Hz pulse, the contents of the counter must be such that it requires only six move pulses for all columns to reach the 1 state. The logical state of the 1-2-4-8 columns of counters J and Q forming the decremental counter would at that instant be J: 1001; Q: 1111.

The arrangement of the logic monitoring the contents of the decremental counter is such that when the logical condition for J and Q stated above are true the logic changes the state of the Last 6 Steps-FF.

This is achieved by monitoring the 1-2-4-8 columns of counter Q and the first and eighth columns of counter J. When all the columns of counter Q reach the 1 state. $\overline{\mathrm{L16S}}$ becomes 0 setting the "K" input of the Last 6 Steps-FF to 0. The "J" input of this flip-flop is simultaneously set to 1 by L16S. Since the reset input of this flip-flop is held at logic 1 by $\overline{\mathrm{DLFZO}}$, the first negative going edge applied to its trigger input while it is in this state will change the state of the flip-flop.

The logical condition of the signal $\overline{\mathrm{L6S}}$ on the trigger input of the last 6 steps-FF is determined by the state of the first and eighth columns of counter J and the signal L16S. As counter J progresses through the final binary count cycle towards the state 1111, a 0 is present in its eighth column up to binary 8 (1000). SMSRD monitoring this column will thus be a 0 up to this point in the final cycle of the counter.

This zero will hold $\overline{\text{L6S}}$ in the 1 state. The instant J reaches binary 9 (1001), both SMSRA and SMSRD become logic 1 which together with the signal L16S (=1) sets $\overline{\text{L6S}}$ to 0.

On the negative going edge of $\overline{\text{L6S}}$ as it is set to 0, the last 6 steps-FF is set to the 1 state. Its output $\overline{\text{L6SF}}$ (=0) sets $\overline{\text{F9SCZO}}$ on the reset input of the first 9 steps counter to 0, clearing the columns of the counter to the zero state. F9SCA and F9SCD are therefore set to 0 which in turn sets $\overline{\text{F9S}}$ to 1 and thus F9S to 0.

$\overline{\text{F9S}}$ (=1) enables the 500 Hz clock pulses (1CP) to pass through the gate on signal line ICPZA whilst simultaneously F9S (=0) prevents any further 1000 Hz clock pulses passing through to the variable clock gate by setting OCPZA to 1 ICPZA (500 Hz) is applied together with OCPZA (=1) and 3CPZA (=1) to a further gate through which the 500 Hz pulses pass. The output of this gate SKCP thus becomes active at 500 Hz. After two inversions, the 500 Hz clock pulses are fed via the variable clock gate on signal line SKCPZC to the binary up/down counter and the decremental counter. The positioning mechanism thus decelerates to a velocity of 500 steps/sec for the final six steps.

A point of interest occuring during the transitionary period when switching from 1000 Hz to 500 Hz is the time delay td shown in the waveform diagrams of fig. The point of interest in the circuit is at the gate generating SKCP since it is at this point that the effect of the delay becomes relevant.

As SKCP goes negative on the fourteenth step of this 20 step seek, it effectively initiates the chain of events leading to $\overline{\text{F9S}}$ being set to 1 - as just described. Due to the cummulative effect of the time delays in this chain of events, there is a finite time delay (td) between the negative going edge of SKCP and the leading edge of $\overline{\text{F9S}}$ as it is set to 1.

The effect of this time delay is dependant upon the phase of the 500 Hz clock with respect to the 1000 Hz clock when the fourteenth variable clock pulse is going negative.

The 500 Hz clock could be going either positive or negative. This is an arbitrary condition and depends upon when the seek is initiated and on the size of the seek. The effect of this time delay when the 500 Hz clock is going positive is to effectively advance the negative going edge of the first 500 Hz variable clock pulse during the last 6 steps. This is illustrated in the following diagrams.

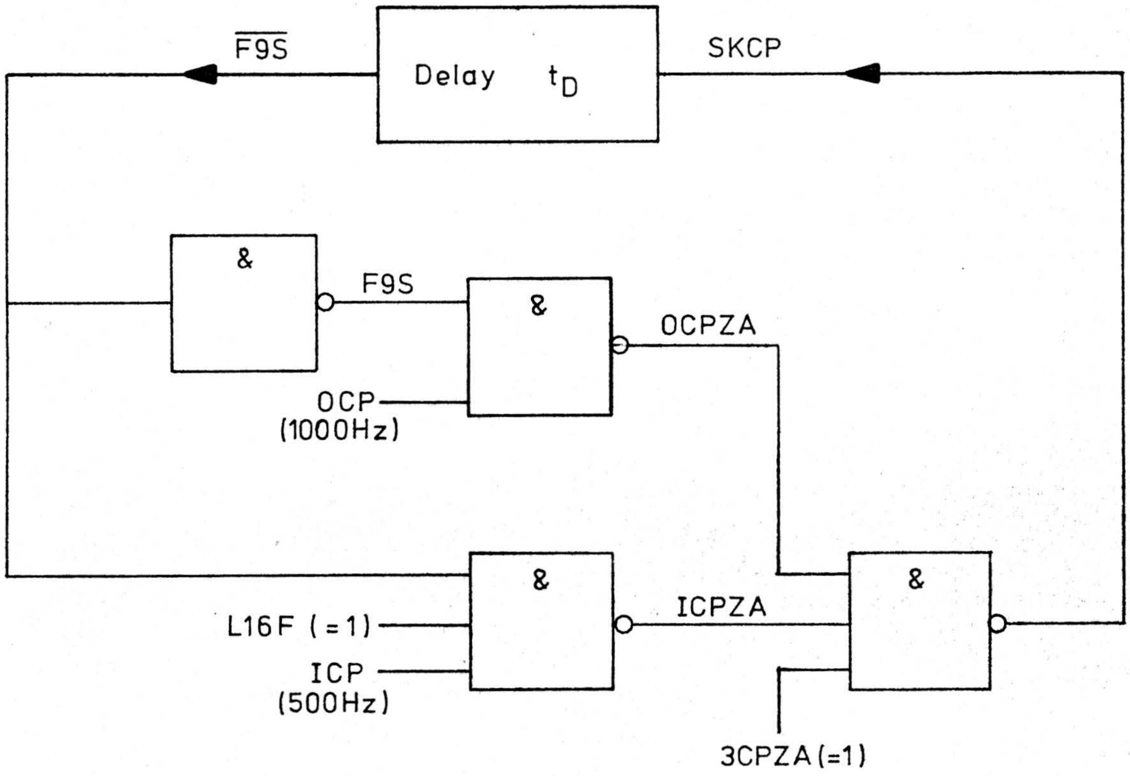


Fig. 3.31 Last 6 Steps Delay Initiation.

When $\overline{F9S}$ goes to logic 1 at time t_D after the fourteenth negative edge of SKCP, all the inputs to the nand gate generating 1CPZA are 1. Thus t_D after the fourteenth negative edge of SKCP, ICPZA becomes 0. SKCP is therefore set back to the 1 state again by ICPZA (=0). Later, when the 500 Hz clock (ICP) goes to 0 again, ICPZA is returned to the 1 state which together with OCPZA (=1) and 3CPZA (=1) sets SKCP to 0, generating the fifteenth negative edge of the variable clock. This edge is clearly advanced as shown in the waveform diagram. The delay t_D has been exagerated in the diagram for descriptive purposes.

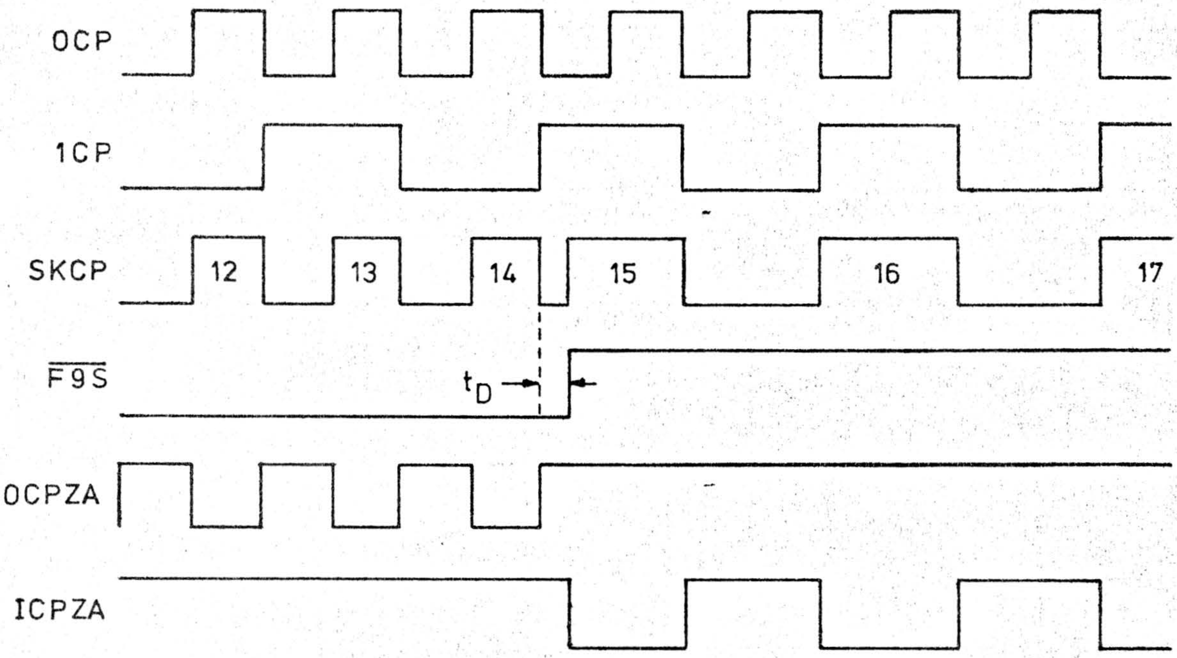


Fig. 3.32 Delay Effect When 1CP is Going Positive

If the 500 Hz clock is going negative on the event of the fourteenth variable clock pulse negative edge, the delay time t_D is ineffective. This is illustrated in the following waveform diagram.

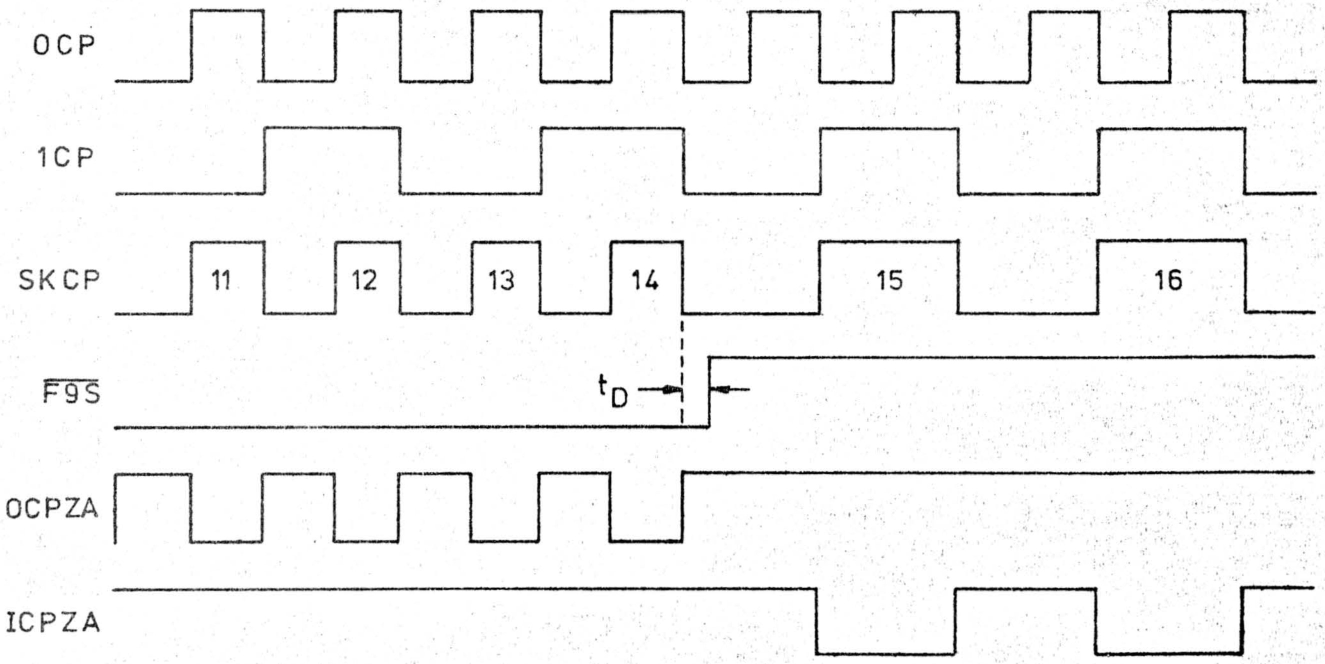


Fig. 3.32 Delay Effect When 1CP is Going Negative

Stopping at the End of the Seek Mission (Fig. 3.29 and 3.30)

On the nineteenth step of this 20 step seek, the positioning mechanism has to move a distance of only one track to reach the required track position. And since the decremental counter has been fed with nineteen variable clock pulses, it requires only one more pulse to bring all columns of the counter to the 1 state. Thus on the negative going edge of the twentieth variable clock pulse SCSRA becomes 1 along with SCSRB, SCSRC and SCSRD. All inputs to the nand gate generating $\overline{SEX}$ are therefore logic 1 setting $\overline{SEX}$ to 0. The instant this occurs $\overline{SEX}$ (=0) causes $\overline{DLFZO}$ to become 0. Due to the cummulative effects of the delays around the circuit, the negative going edge of DLFZO lags the negative going edge of the twentieth variable clock pulse. This delay is exagerated in the waveform diagram (Fig. 3.30) for descriptive purposes.

When $\overline{DLFZO}$ becomes 0, it simultaneously sets the following flip-flops to the conditions indicated:

(a) Less than 16 steps-FF (L16F=0, $\overline{L16F}$=1)
(b) Seek-FF (SKF=0)
(C) Direction Loaded (DLF=0, $\overline{DLF}$=1)

When the Less Than 16 Steps-FF is reset to the zero state, its output L16F (=0) inhibits any further 500 Hz clock pulses being fed to the variable clock gate by setting ICPZA to logic 1.

$\overline{L16F}$ (=1) however, enables the 125 Hz clock pulses to pass through the gate generating 125 Hz at the variable clock gate. But since $\overline{DTCZC}$ (=0) has also reset the Seek-FF to the zero state, SKF (=0) inhibits the variable clock gate by setting $\overline{SKCPZC}$ to logic 1. Thus although the 125 Hz clock pulses are present at the input to the variable clock gate, they cannot pass through it.

Since the variable clock gate is shut, the condition of the binary up/down counter, remains that set by the twentieth variable clock pulse. Thus the condition of the stepping motor control windings also remain the same - as set by the binary up/down counter. The positioning mechanism is therefore aligned over the required track position. But due to the momentum of the moving parts overshoot and oscillation about this final track position occurs - as has already been discussed for arrival at track 000.

To ensure that these oscillations have decayed to zero before releasing a detent pawl onto the rack and locking the positioning mechanism in position the 24ms delay circuit is initiated. This is effected by the Direction Loaded-FF.

24ms Delay (Fig. 3.19)

When $\overline{\text{DLFZO}}$ (=0) sets the Direction Loaded-FF to the zero state, its output $\overline{\text{DLF}}$ (=1) along with $\overline{\text{DTT}}$ (=1) and REL3CP (=1) sets DTCZO to logic 0. $\overline{\text{DTT}}$ is a test input and is normally held in the 1 state.
DTCZO (=0) is inverted setting $\overline{\text{DTCZO}}$ to 1. The state of $\overline{\text{DTCZO}}$ prior to reset of the Direction Loaded-FF was logic 0. The Detent-FF has therefore been held in the zero state by this signal ($\overline{\text{DTCZO}}$ = 0). Signal $\overline{\text{DETP}}$; defined by DTCZO (=0) and the Detent-FF output $\overline{\text{DETF}}$ (=1), is thus maintained logic 1. Whilst this signal is in the 1 state, both pawls remain retracted.

$\overline{\text{DTCZO}}$ (=1) initiates the 24ms delay circuit. The operation of this delay has already been discussed - see the OFF-LINE section of this book. At the end of the 24ms delay, the Detent-FF is reset to the 1 state. Its output $\overline{\text{DETF}}$ (=0) along with DTCZO (=0) sets $\overline{\text{DETP}}$ to 0.

The instant $\overline{\text{DETP}}$ is set to the 0 state, one of the detent pawls is released onto the rack. The binary up/down counter output SMCA defines which pawl is released. If SMCA is 0 $\overline{\text{DETDIE}}$ becomes logic 1 and the even pawl is released onto the rack. Conversely when SMCA is 1, $\overline{\text{DETDZE}}$ becomes logic 1 and the odd pawl is released.

The condition of the binary up/down counter when the positioning mechanism is at track 000 is 0000. And after 16 steps forward its condition becomes 1111. Thus after a total of 20 steps forward, the counter goes through one complete count cycle from 0000 to 1111, resets to 0000 again, and then counts a further four steps to the condition 0100.The condition of its first column is thus a 0. And clearly will always become 0 whenever the seek mission is an even number of steps forward or reverse. Since SMCA monitors the first column of the counter it will be in the 0 state. The even pawl will therefore be released.

40ms after DTCZO has been set to 0, outputs DTCB and DTCD of the 24/40 ms delay counter become 1 causing the Seek Complete-FF to be reset to the 1 state. Output $\overline{\text{SKCF}}$ (=0) of this flip-flop, is fed to the stepmotor drive circuits, inhibiting the output gates and results in the stepmotor control winding being de-energised.

SKCF (=1) causes the Head on Track signal (Seek Complete) $\overline{\text{H0TZB} *}$ to be set to 0 informing the control unit that the X1210 is available to implement the read, write or eraze instructions.

A Seek Mission of Less than 16 Steps

For a seek of less than 16 steps, the variable clock frequency is held constant at 125 Hz throughout the complete mission. The positioning mechanism therefore moves at a constant 125 step/sec during the seek.

Consider as an example a seek reverse of 2 steps.

Input Signals (Fig. 3.27 and 3.28)

A seek mission of two steps reverse would be initiated by:

(a) Activating the $\overline{\text{BUS1} *}$ channels simultaneous with the TAG1 * channel. This contains the instructions to move by 2 steps.

(b) Activating the $\overline{\text{BUS5} *}$ and $\overline{\text{TAG3} *}$ channels (when the $\overline{\text{TAG1} *}$ channel has been de-activated). This constitutes the instructions to move reverse.

When the difference select instructions are received, the $\overline{\text{BUS1} *}$ and $\overline{\text{TAG1} *}$ channels are set to logic 0. These signals are inverted by the transmitter/receiver circuits on card 12, setting the signals BUS1 and TAG1 to logic 1. These two signals are in turn inverted setting $\overline{\text{BUS1ZA}}$ and $\overline{\text{TAG1ZA}}$ at the input to the decremental counter to logic 0.

When the negative going edge of the TAG1 pulse is applied to the strobe input of counter J, the zero present on its $\overline{\text{BUS1ZA}}$ input is transfered to the second column of the counter. The state of the counter has thus been set to 1101. Since all inputs to counter Q are 1 the state of counter Q remains at 1111.

The signal SMSRB monitoring the second column of counter J thus becomes 0 setting $\overline{\text{SEX}}$ to logic 1. And since the signals $\overline{\text{TSKINH}}$, $\overline{\text{MC}}$ and $\overline{\text{USFZA}}$ controlling the state of DLFZO along with $\overline{\text{SEX}}$ are also logic 1, DLFZO is set to 0 causing $\overline{\text{DLFZO}}$ to become logic 1. $\overline{\text{DLFZO}}$ (=1) removes the dominant 0 from the reset inputs of the Less Than 16 Steps-FF, the Last 6 Steps-FF and the Seek-FF. This removes the inhibit from these flip-flops and enables them to be set or reset accordingly.

Recognition of a Less Than 16 Steps Seek (Fig. 3.34)

When no difference select data is supplied on the BUS4, BUS5, BUS6 and BUS7 lines all columns of counter Q remain in the 1 state after the event of the TAG1 pulse. The signals SCSRE, SCSRF, SCSRG and SCSRH monitoring the four columns of counter Q thus remain at logic 1. This maintains $\overline{\text{L16S}}$ on the 'D' input of the Less Than 16 Steps-FF at logic 0. Thus when the positive going edge of the TAG1 pulse is applied to the trigger input of this flip-flop, it remains in the zero state (L16F=0, $\overline{\text{L16F}}$=1).

Inhibiting The 500 Hz Clock (Fig. 3.34)

The Less Than 16 Steps-FF output signal L16F (=0) is applied along with the 500 Hz clock pulses to a nand gate, setting the gate output signal ICPZA to logic 1.

Inhibiting the 1000 Hz Clock (Fig. 3.34)

L16F (=0) also sets the reset input of the first nine steps counter to 0. The columns of the counter are thus cleared to 0. Signals F9SCA and F9SCD monitoring the first and eighth columns of this counter are therefore both in the zero state. This sets $\overline{\text{F9S}}$ to logic 1 causing F9S to become 0. F9S (=0) is applied together with the 1000 Hz clock to a nand gate, setting its output signal OCPZA to 1.

Enabling the 125 Hz Clock (Fig. 3.34)

$\overline{\text{L16F}}$ (=1) is applied together with the 125 Hz clock pulses (3CP) to a nand gate enabling the clock pulses to pass through the gate on signal line 3CPZA. This signal is applied together with OCPZA (=1) and 3CPZA (=1) to a further nand gate enabling the 125 Hz pulses to pass through the gate on signal line SKCP. After two inversions the 125 Hz clock (SKCZB) is applied to the input of the variable clock gate and also to the trigger input of the Seek-FF. This flip-flop is in the zero state however. Its output SKF (=0) prevents the the 125 Hz clock passing through the gate. The Seek-FF is maintained in this condition until the control select instructions are received by the X1210.

Instructions To Reverse (Fig. 3.28 and 3.34)

The instructions to move in the reverse direction are received when the BUS5 * and TAG3 * channels on card 12 are set to 0.

These signals are inverted by the transmitter/receiver circuits setting the BUS5 and TAG3 signals to 1, BUS5 (=1) and TAG3 (=1) are applied to a nand gate causing its output $\overline{FWDFZO}$ to become logic 0.

$\overline{FWDFZO}$ (=0) performs two functions. It resets the Forward-FF to the zero state. And it also resets the Direction Loaded-FF to the 1 state.

The Forward-FF output $\overline{FWDF}$ (=1) together with $\overline{SKINH}$ (=1) sets SKFWD to logic 0 causing the U/$\overline{D}$ input signal ($\overline{SMCUP}$) to the up/down counter to become 0. The cyclic rotation of the binary up/down counter is thus set to count down in the direction 1111 to 0000. And when the counter is cycled in this direction, the direction of rotation of the positioning mechanism is towards track 000.

Enabling the Variable Clock Gate (Fig. 3.34)

The Direction Loaded-FF output DLF (=1) removes the dominant 0 from the 'D' input of the Seek-FF. And since the reset input of this flip-flip has already been set to 1 by the difference select instructions (DLFZO=1), its state will be altered by the first positive going edge on its trigger input. The 125 Hz clock pulses SKCZB have been present on the input to the variable clock gate and also on this trigger input since the positive going edge of the TAG1 pulse. Thus the first positive going edge of the 125 Hz clock on the Seek-FF trigger input occuring after the Direction Loaded-FF is set to the 1 state causes the Seek-FF to be set to the 1 state (SKF=1).

The instant SKF becomes 1, the 125 Hz pulses pass through the gate on signal line $\overline{SKCPZC}$ and after inversion, on SKCPZC to the trigger input of the decremental counter and also via the gating circuits to the trigger input of the binary up/down counter.

The 125 Hz variable clock pulses have to pass through two nand gates before they can be fed into the trigger input of the up/down counter. The first gate is controlled by the seek inhibit signal $\overline{SKINH}$ and the signal $\overline{REL3CP}$. Unless an unsafe condition arises $\overline{SKINH}$ remains in the 1 state throughout on-line operation of the X1210. $\overline{REL3CP}$ is also at logic 1. It is set to this condition by $\overline{RTZF}$, $\overline{RTRP}$ and $\overline{CLCY}$ all of which are at logic 1. Furthermore, they like $\overline{SKINH}$ remain in the 1 state throughout on-line operation. Thus since both $\overline{SKINH}$ and $\overline{REL3CP}$ are 1, the 125 Hz pulses pass through the gate on signal line 3CPP to the input of the second nand gate.

This gate is controlled by SKCCP. And SKCCP is in turn controlled by REL3CP. Since REL3CP is set to the 0 state by $\overline{\text{RTZF}}$ (=1), $\overline{\text{RTRP}}$ (=1) and $\overline{\text{CLCY}}$ (=1), then SKCCP is set to the 1 state. The 125 Hz pulses therefore pass through this second nand gate on line SMCCP to the trigger input of the binary up/down counter. And since the U/$\overline{\text{D}}$ input of the counter has already been set to logic 0 by the Forward-FF, the positioning mechanism steps backwards on each negative edge of the 125 Hz clock. At the same time the 125 Hz clock is also fed into the decremental counter. The initial state of the decremental counter has been set to 1101. The counter responds to the negative going edges of the variable clock. Thus, on the second negative going edge of the 125 Hz the state of the decremental becomes 1111, whilst the positioning mechanism makes its second step backwards and reaches the required track position.

Completion of Seek Mission (Fig. 3.34)

When signals SCSRA, SCSRB, SCSRC and SCSRD monitoring the 1-2-4-8 columns of counter Q all become 1, $\overline{\text{SEX}}$ is set to logic 0. $\overline{\text{SEX}}$ (=0) causes $\overline{\text{DLFZO}}$ to become 0. And $\overline{\text{DLFZO}}$ (=0) resets the Direction Loaded-FF to the 1 state. The Direction Loaded-FF output DLF (=0) and $\overline{\text{DLF}}$ (=1) initiates two functions.

DLF (=0) sets the 'D' input of the Seek-FF to logic 0 causing the flip-flop to be reset to the zero state. The Seek-FF output SKF (=0) thus sets the output of the variable clock gate $\overline{\text{SKCPZC}}$ to logic 1, preventing any further 125 Hz pulses passing through it. Since the variable clock gate is shut, the condition of the binary up/down counter remains that set by the second 125 Hz clock pulse. The stepping motor control windings in turn remain energised in the condition as set by the up/down counter. The positioning mechanism has therefore been moved backwards by two tracks on the magnetic disk and is thus aligned over the required track position.

Initiating the 24/40ms and Releasing a Pawl (Fig. 3.19)

Due to the momentum of the moving parts overshoot and oscillation about the final track position occurs - as has already been discussed for arrival at track 000. To ensure that these oscillations have decayed to zero before releasing a detent pawl onto the rack and locking the positioning mechanism into position, the 24/40ms delay circuit is initiated. This is effected by the Direction Loaded-FF output $\overline{\text{DLF}}$ (=1).

The subsequent operation of the delay circuit and the release of a detent pawl has already been discussed for the end of a greater than 16 steps seek mission - which is identical - and thus will not be repeated here.

HEAD SELECTION (Fig. 3.28)

To select the upper head, the Control unit momentarily sets the $\overline{\text{TAG 2 *}}$ and $\overline{\text{BUS 0}}$ * channels to zero. Both these signals are inverted causing the TAG 2 and BUS 0 signals to the write-eraze amplifier on card 6 to be momentarily set to logic 1. Conversely, to select the lower head, only the TAG 2 channel is set to logic 0. The head select signals to card 6 under these conditions are thus: TAG 2 = logic 1; BUS 0 = logic 0.
Further details concerning how these two signals implement head selection is discussed in the Electronics section Volume 5.

READ, WRITE OR ERAZE ENABLE (Fig. 3.28)

The read, write or eraze enable instructions are initiated by the control unit when it has received the Head on Track signal (On Cylinder) from the X1210.

Read Enable

The read enable instruction is effected when the control unit momentarily sets both the $\overline{\text{TAG 3 *}}$ and $\overline{\text{BUS 1 *}}$ channels to logic 0. Both these signals are inverted setting BUS 1 and TAG 3 to logic 1 at the input to the nand gate generating the read enable signal $\overline{\text{RDEN}}$. This signal ($\overline{\text{RDEN}}$) is thus set to the zero state and applied to the clock/speed 0 circuits on card 7. The effects of this are fully discussed in the Electronics section in Volume 5.

Write Enable

The write enable instruction is effected when the control unit momentarily sets both the $\overline{\text{TAG 3 *}}$ and $\overline{\text{BUS 0 *}}$ channels to logic 0. Both these signals are inverted setting BUS 0 and TAG 3 to logic 1 at the input to the nand gate generating the write enable signal WREN. This signal is thus set to the zero state and applied to the clock/speed 0 circuits on card 7 and to the write-eraze amplifier on card 6. The effects of this are fully discussed in the Electronics section in Volume 5.

Eraze Enable

The eraze enable instruction is effected when the control unit momentarily sets both the $\overline{\text{TAG 3 *}}$ and $\overline{\text{BUS 4 *}}$ channels to logic 0.

Both these signals are inverted setting TAG 3 and BUS 4 to logic 1 at the input to the nand gate generating the eraze enable signal $\overline{\text{EREN}}$. This signal is thus set to the zero state and applied to the clock/speed 0 circuits on card 7 and to the write-eraze amplifier on card 6. The effects of this are fully discussed in the Electronics section in Volume 5.

RETURN TO ZERO (Fig. 3.16)

If due to some transient fault condition incorrect data should be read from the magnetic disk, the computer system will recognise that it has received the wrong data and will inform the control unit to instruct the positioning mechanism to return to track 000. When it has been returned to track 000, the control unit can be up-dated to this reference position (T000). The seek mission can then be repeated to gain access to the relevant data.

The instructions to return to zero are initiated by momentarily setting the $\overline{\text{TAG 3 *}}$ and $\overline{\text{BUS 6 *}}$ channels to logic 0. This causes the return to zero signal to be set to logic 0. $\overline{\text{RTZFZ1}}$ (=0) sets the Return to Zero-FF to the 1 state causing the positioning mechanism to retract back towards track 000 at 125 steps/sec. The circuit operation is identical to that shown in Fig. 3.16.

STOPPING THE X1210 (Fig. 3.15)

While the X1210 is on-line the Start-FF is in the 1 state. When the start/stop button is pressed to stop the X1210, signals $\overline{\text{SSU *}}$ and $\overline{\text{SSD *}}$ are inverted for the duration of pressing the button. $\overline{\text{SSU *}}$ momentarily becomes logic 1 and $\overline{\text{SSD *}}$ logic 0. $\overline{\text{SSD *}}$ (=0) in turn momentarily changes the state of SSDF and $\overline{\text{SSDF}}$; $\overline{\text{SSDF}}$ going to logic 0 and SSDF to logic 1. Since the signal $\overline{\text{STFZO}}$ on the reset input of the Start-FF is logic 1, the state of this flip-flop will be changed by the first positive going edge on its trigger input. Thus when the start/stop button is released and $\overline{\text{SSDF}}$ goes back to logic 1 again, its positive going edge changes the Start-FF to the zero state (STF=0, $\overline{\text{STF}}$=1). The instant this occurs, signal STF (=0) initiates three functions. It causes the heads to be retracted from the disk, the disk drive motor to be stopped and the positioner to move to the fully retracted position.

Retracting the Read-Write Heads (Fig. 3.35)

STF (=0) causes the head valve energised signal $\overline{HVE}$ to become logic 1. $\overline{HVE}$ (=1) is applied to the valve driver and level shifter circuit on card 3 causing the base-emitter diode of transistor TS9 to be reverse biased. This turns TS9 off. The base voltage of transistor TS10 thus falls to 0V causing TS10 to turn off. The collector of TS10 thus rises to a positive voltage level, setting the signal $\overline{HVA}$ * to logic 1. $\overline{HVA}$ * (=1) de-energises the head valve solenoid causing the valve to shut. The pneumatic supply to the head assemblies is thus removed, causing the read-write heads to be retracted from the disk surface and the nylon cleaning brushes to be lowered into position.

The collector voltage level of TS10 causes the common anode point of diodes GR1 and GR2 to rise. This forward biases GR2, causing it to conduct. The resultant dc voltage developed across R24 forward biases the base-emitter diode of transistor TS11, driving it into the conduction region. The output signal H0D on the collector of TS11 thus falls to logic 0 setting H0D to 1.

Stopping the Disk Drive Motor (Fig. 3.35)

When the Start-FF output STF becomes logic 0 it sets $\overline{PMEP}$ to 1. And $\overline{PMEP}$ (=1) together with the signal $\overline{H0D}$ (=1) sets PME to 0. $\overline{PME}$ is thus set to 1. $\overline{PME}$ (=1) causes transistors TS7 and TS8 in the relay driver circuit to be turned off. The output signal $\overline{HVA}$ * on the collector of TS8 thus becomes logic 1 causing the switching unit relay to be de-energised. Thus, since the disk drive motor 220v ac supplies are fed to the motor via the contacts of this relay, the motor is de-energised, decelerates and stops.

Complete Retraction of the Positioning Mechanism (Fig. 3.35)

STF (=0) sets $\overline{PMEP}$ to logic 1. And PMEP (=1) along with H0D (=1) and $\overline{R}$ (=1) causes the return to retract signal $\overline{RTRP}$ to become logic 0. RTRP (=0) sets $\overline{SMCUP}$ to logic 0 and REL3CP to logic 1. REL3CP enables the 125 Hz clock pulses to pass through the nand gate generating SKCPP to a further gate controlled by signal 3CPP. This latter signal is set to the 1 state indirectly by STF (=0). Since STF (=0) sets $\overline{HVE}$ to 1. And HVE (=0) sets $\overline{SKINH}$ to logic 0. $\overline{SKINH}$ in turn sets 3CPP to logic 1. The 125 Hz pulses thus pass through the second gate on SMCPP to the trigger input of the binary up/down counter. Since the signal $\overline{SMCUP}$ has set the U/$\overline{D}$ input of the up/down counter to logic 0 the counter commences counting through the binary progression states in direction 1111 to 0000. This causes the stepping motor to drive the positioner at a velocity of 125 steps/sec out of the cartridge towards the retracted position.

When the positioner reaches the retracted position, it opens the retract micro-switch causing R * to be set to logic 1. R * (=1) sets $\overline{R}$ to 0. And $\overline{R}$ (=0) sets the return to retract signal $\overline{RTRP}$ to 1. The three inputs to the gate generating REL3CP, namely $\overline{RTRP}$, $\overline{RTZF}$ and $\overline{CLCY}$ are thus all logic 1 setting REL3CP to the zero state. REL3CP (=0) prevents any further 125 Hz clock pulses being fed to the up/down counter by setting SKCCP to logic 1. Thus, the instant the positioner opens the retract micro-switch the 125 Hz clock to the counter is stopped and the condition of the counter remains set to that condition as defined by last 125 Hz pulse to be fed into the counter. The stepping motor windings therefore remain energised in the condition corresponding to that of the up/down counter, locking the rotor and thus the positioner into position and holding the micro-switch open.

SPECIAL CONDITIONS

THE UNSAFE CONDITIONS

The X1210 safety logic is initiated when either one or more of the following incompatible conditions occur:

(a) Both read-write heads are selected.

(b) Write current without write enable.

(c) Read, write or eraze enable simultaneously.

(d) Write data but [illegible] ac write current.

(e) Eraze current but no write enable

(f) Write enable but no eraze current.

(g) Write or eraze driver enabled before Head on track (On Cylinder) signal has been generated.

(h) Disk drive motor stopped or speed incorrect.

(i) Overshoot of track 000 towards the retracted position or overshoot of track 205 (towards disk centre) whilst on a seek mission.

Read-Write OK (Fig. 3.36)

Conditions (a) to (g) inclusive are monitored by the Safety/supply/clock/speed 0 card 7. Complete details concerning how these conditions are checked is discussed in the Electronics section Volume 5. Whenever one of the fault conditions (a) to (g) occurs, card 7 sets the read-write OK signal signal RDWRK to logic 0 and initiates the safety logic.

Disk Drive Motor Slow or Stopped (Fig. 3.36)

Condition (h) is checked by monitoring the speed OK signal SPKF. When the disk drive motor is running at the correct speed SPKF is at logic 1. The instant the disk speed slows or stops however SPKF becomes logic 0

Track-1 (Fig. 3.5 and 3.36)

Overshoot of track 000 towards the retracted position is checked by monitoring signal $\overline{\text{HU000}}$. Overshoot of the track 000 position is defined by signals SMCA, $\overline{\text{2S1415}}$ (see Fig. 3.5) and $\overline{\text{OPZ}}$. These signals control the logical state of $\overline{\text{HU000}}$.

With reference to the truth table on Fig 3.5 and the circuit of Fig 3.36 it can be seen that if the positioner moves by one track towards the retracted position the condition of the binary up/down counter is 1111, SMCA is therefore 1. It can also be seen from the truth table that $\overline{\text{2S1415}}$ for this condition is at logic 0. Thus since $\overline{\text{OPZ}}$ is at logic 0 the output of the nor gate generating $\overline{\text{HU000P}}$ becomes logic 1. $\overline{\text{HU000P}}$ (=1) is applied together with SMCA (=1) to a nand gate setting its output signal $\overline{\text{HU000}}$ to logic 0. And when $\overline{\text{HU000}}$ becomes logic 0, the safety logic is initiated.

Track 204 (Fig. 3.16 and 3.36)

The position of track 204 is defined by two variables. These are the state of the track 200 micro-switch and the logical state of the encoding logic signal $\overline{\text{IS12}}$. When the track 200 micro-switch is opened and shortly afterwards $\overline{\text{IS12}}$ becomes a 0, $\overline{\text{IS12}}$ (=0) and $\overline{\text{H0203}}$ (=0) combine to set the track 204 signal T204 to logic 1. This signal is inverted setting $\overline{\text{T204}}$ to zero at the input to the safety logic.

Operation of the Safety Logic (Fig. 3.36)

The input to the safety logic can be considered to be at the input of the nand gate generating signal US. This is because the input signals to this gate; RDWRK, SPKF, $\overline{\text{HU000}}$ and $\overline{\text{T204}}$ define each of the unsafe conditions discussed.

When all conditions are safe, each of the input signals to this gate are at logic 1 setting signal US to 0. US (=0) causes $\overline{\text{USFZ1}}$ at the input to the Unsafe-FF to be held at logic 1. Whilst this condition exists the state of the unsafe-FF remains in the zero state (USF =0, USF =1), as defined by the master clear pulse.

If an unsafe condition developed - say for example the disk drive motor ran slow - SPKF would become logic 0 setting US to logic 1. When the machine has been started both STF and $\overline{\text{SCSFZA}}$ are at logic 1. Thus US (=1) STF (=1) and $\overline{\text{SCSFZA}}$ (=1) combine to set $\overline{\text{USFZ1}}$ to zero at the input to the Unsafe-FF. This resets the flip-flop to the one state (USF=1; $\overline{\text{USF}}$=0). The instant this occurs USF (=1) initiates two functions. USF (=1) is fed to the transmitter/receiver card 12 and after inversion is applied to the control unit informing it that an unsafe condition exists within the X1210. This prevents the computer system sending further write data to the X1210 thus preserving the integrity of the information.

The second function initiated by the reset state of the Unsafe-FF (USF = 1) is to set the seek inhibit signal $\overline{\text{SKINH}}$ to logic 0. $\overline{\text{SKINH}}$ (=0) prevent any further variable clock pulses being fed to the up/down counter and thus stops the positioning mechanism. This is particularly relevant to the two possible track overshoot conditions at 'track-1' and track 204. Since for either of these conditions, if the positioner were not stopped damage to the read-write heads would inevitably result.

Turn On Clear Period - Positioner Not Fully Retracted (Fig. 3.14)

If the positioning mechanism were not fully retracted and the power supplies to the X1210 were switched on, the logic automatically guides the positioning mechanism back to the fully retracted position.

The instruction to retract is initiated by the retract micro-switch. When the positioner is not fully retracted the micro-switch is closed setting $\overline{\mathrm{R}}$ to logic 1. During the TOC period the Start-FF is set to the zero state. Its output STF (=0) sets $\overline{\mathrm{PMEP}}$ to logic 1. The head on disc signal $\overline{\mathrm{H0D}}$ during this period is also in the 1 state. $\overline{\mathrm{R}}$ (=1), $\overline{\mathrm{PMEP}}$ (=1) and $\overline{\mathrm{H0D}}$ (=1) combine to set the return retract signal $\overline{\mathrm{RTRP}}$ to logic 0.

$\overline{\mathrm{RTRP}}$ (=0) is fed to the stepmotor/detent control card 8 setting the $\mathrm{U}/\overline{\mathrm{D}}$ input of the up/down counter to logic 0. $\overline{\mathrm{RTRP}}$ (=0) also sets REL3CP to logic 1. $\overline{\mathrm{REL3CP}}$ (=1) enables the 125 Hz clock pulses to pass to the trigger input of the up/down counter. And since the $\mathrm{U}/\overline{\mathrm{D}}$ has been set to logic 0, the cyclic rotation of the counter is in the direction 1111 to 0000. The positioner thus retracts at a velocity of 125 steps/sec.

The instant the positioner reaches the fully retracted position and opens the micro-switch $\overline{\mathrm{R}}$ is set to logic 0 causing the return to retract signal $\overline{\mathrm{RTRP}}$ to become logic 1. The positioner thus stops.

Power Supply Failure While in the Cartridge

If the power supplies were to fail while the positioner is in the cartridge, the cartridge can be removed from the X1210 as discussed in the Operators Book Volume 2. If the power failure is due to some minor fault condition however and the power supplies can be re-applied within a relatively short period of time the emergency removal procedure is un-necessary.

If the supplies are re-applied while the cartridge is still in the pack the positioner will immediately commence moving towards the retracted position. But if the start/stop button is pressed before the positioner is out of the cartridge, the positioner simultaneously reverses and commences the cleaning cycle from the point of reversal ie if the button is pressed whilst the positioner is retracting and at that precise instant it is moving over track 100, the cleaning cycle commences from track 100

<h2>IDENTIFICATION</h2>

All inter-connections between the logic cards discussed in this book and between the cards and wiring loom are shown in Fig. 3.37.

SIGNAL NAMES

The logic signal names used on the cards described in this book are as follows:

000	INTERNAL GROUND
005	+ 5V
006	- 6V
012	+12V
012	-12V
024	+24V
OCP	1000Hz CLOCKPULSE
OCPZA	" "
1CP	500Hz CLOCKPULSE
1CPZA	" "
1S00	ONES GROUP STATE 00
1S02	" " " 02
1S04	" " " 04
1S06	" " " 06
1S08	" " " 08
1S10	" " " 10
1S12	" " " 12
1S14	" " " 14
2CP	250Hz CLOCKPULSE
2S0001	TWOS GROUP STATES 00 AND 01
2S0203	" " " 02 " 03
2S0405	" " " 04 " 05
2S0607	" " " 06 " 07
2S0809	" " " 08 " 09
2S1011	" " " 10 " 11
2S1213	" " " 12 " 13
2S1415	" " " 14 " 15
3CP	125Hz CLOCKPULSE
3CPP	" " - PREPARATION
3CPZA	125Hz CLOCKPULSE
4S0003	FOURS GROUP FROM STATE 00 TO 03
4S0407	" " " " 04 " 07
4S0811	" " " " 08 " 11
4S1215	" " " " 12 " 15

SDU 20 SIGNAL-NAMES

BUS 0	BUSLINE 0
BUS 0ZA	" 0
" 1	" 1
" 1ZA	" 1
" 2	" 2
" 2ZA	" 2
" 3	" 3
" 3ZA	" 3
" 4	" 4
" 4ZA	" 4
" 5	" 5
" 5ZA	" 5
" 6	" 6
" 6ZA	" 6
" 7	" 7
" 7ZA	" 7
C1E	COIL 1 ENERGISED
C2E	" 2 "
C3E	" 3 "
C4E	" 4 "
C5E	" 5 "
C6E	" 6 "
C7E	" 7 "
C8E	" 8 "

C1P	COIL 1 ENERGISED
C2P	" 2 "
C3P	" 3 "
C4P	" 4 "
C5P	" 5 "
C6P	" 6 "
C7P	" 7 "
C8P	" 8 "

CD1E	COILDRIVER 1 ENERGISED
CD2E	" 2 "
CD3E	" 3 "
CD4E	" 4 "
CD5E	" 5 "
CD6E	" 6 "
CD7E	" 7 "
CD8E	" 8 "

CD1P	COILDRIVER 1 PREPARATION
CD2P	" 2 "
CD3P	" 3 "
CD4P	" 4 "
CD5P	" 5 "
CD6P	" 6 "
CD7P	" 7 "
CD8P	" 8 "

SDU 20 SIGNAL-NAMES

CLCY	CLEANING CYCLE
CLF	CLEANING-FF
CLFZA	" "
CP	CLOCK-PULSE FROM TEST OSCILLATOR
CPDS5	CLOCK-PULSE DIVIDER STROBE
CPSB	CLOCK-PULSE GENERATOR STROBE
DET1E	DETENT 1 ENERGISED
DET1P	" 1 POWER
DET2E	" 2 ENERGISED
DET2P	" 2 POWER
DETD1E	" -DRIVER 1 ENERGISED
DETD2E	" – " 2 "
DETF	" -FF
DETFZ1	" -FF SET
DETP	" PREPARATION
DLF	DIRECTION-LOADED-FF
DLFZO	" " FF-RESET
DTCA	DELAY-TIME-COUNTER A
DTCB	" " " B
DTCC	" " " C
DTCD	" " " D
DTCSB	" " " STROBE
DTCZO	" " " RESET
DTT	DELAY-TIME-TEST
EREN	ERASE-ENABLE
EXD	EXCHANGE-DISK
EXDL0N	" – " -LAMP ON
F9S	FIRST-NINE-STEPS
F9SCA	" " " COUNTER A
F9SCCP	" " " " CLOCK PULSE
F9SCD	" " " " B
F9SCSB	" " " " STROBE
F9SCZO	" " " " RESET
FWDF	FORWARD-FF
FWDFZO	" " RESET
FWDFZ1	" " SET
H0200	HEAD OVER 200
H0D	HEAD ON DISK
H0DZA	" " "
H0T	HEAD ON TRACK
H0TZA	" " "
H0TZB	" " "
HU000	HEAD UNDER TRACK 000
HU000P	" " " " PREPARATION
HVA	HEAD-VALVE-ACTIVATED
HVE	" " ENERGISED
IOO5	INPUT OVER RESISTOR CONNECTED TO + 5V

SDU 20 SIGNAL-NAMES

IP	INDEX-PULSE
IPDF	INDEX-PULSE -DIVIDER-FF
IPZA	INDEX-PULSE
ISI	INDEX SECTOR-INPUT
ISM	INDEX SECTOR-MONOSTABLE
IS0	INDEX SECTOR-OUTPUT
ISP	" " -PULSE
L16F	LESS THAN 16 STEPS-FF
L16S	LESS THAN 16 STEPS
L6S	LAST 6 STEPS
L6SF	" " " -FF
MC	MASTER CLEAR
0PZ	OPTICAL ZERO
PME	PACKMOTOR ENERGISED
PMEP	" ENERGISING PREPARATION
PMRA	" RELAY ACTIVATED
PMSP	" START PREPARATION
R	RETRACTED
RDDA	READ DATA
RDEN	READ ENABLE
RDWRK	READ-WRITE-OK
REL3CP	RELEASE 125 Hz
RT0	READY TO OPERATE
RT0ZA	READY TO OPERATE
RT0ZB	" " "
RTRP	RETURN TO RETRACT POSITION
RTZ	RETURN TO ZERO
R TZF	" " " -FF
RTZFZA	" " " "
RTZFZ1	" " " " -SET 1
RTZFZ2	" " " " -SET 2
SCSRA	STEP-COUNTER-STORAGE-REGISTER A
SCSRB	" " " " B
SCSRC	" " " " C
SCSRD	" " " " D
SCSRE	" " " " E
SCSRF	" " " " F
SCSRG	" " " " G
SCSRH	" " " " H
SCSRZO	" " " " "-RESET
SEX	STEPS EXECUTED
SKCF	SEEK COMPLETE-FF
SKCFZO	" " "-RESET
SKCFZ1	" " "-SET
SKCP	SEEK CLOCKPULSE
SKCPP	SEEK CLOCKPULSE PREPARATION
SKCPZA	" " "
SKCPZB	" " "
SKCPZC	" " "
SKCPZD	" " "
SKF	SEEK-FF

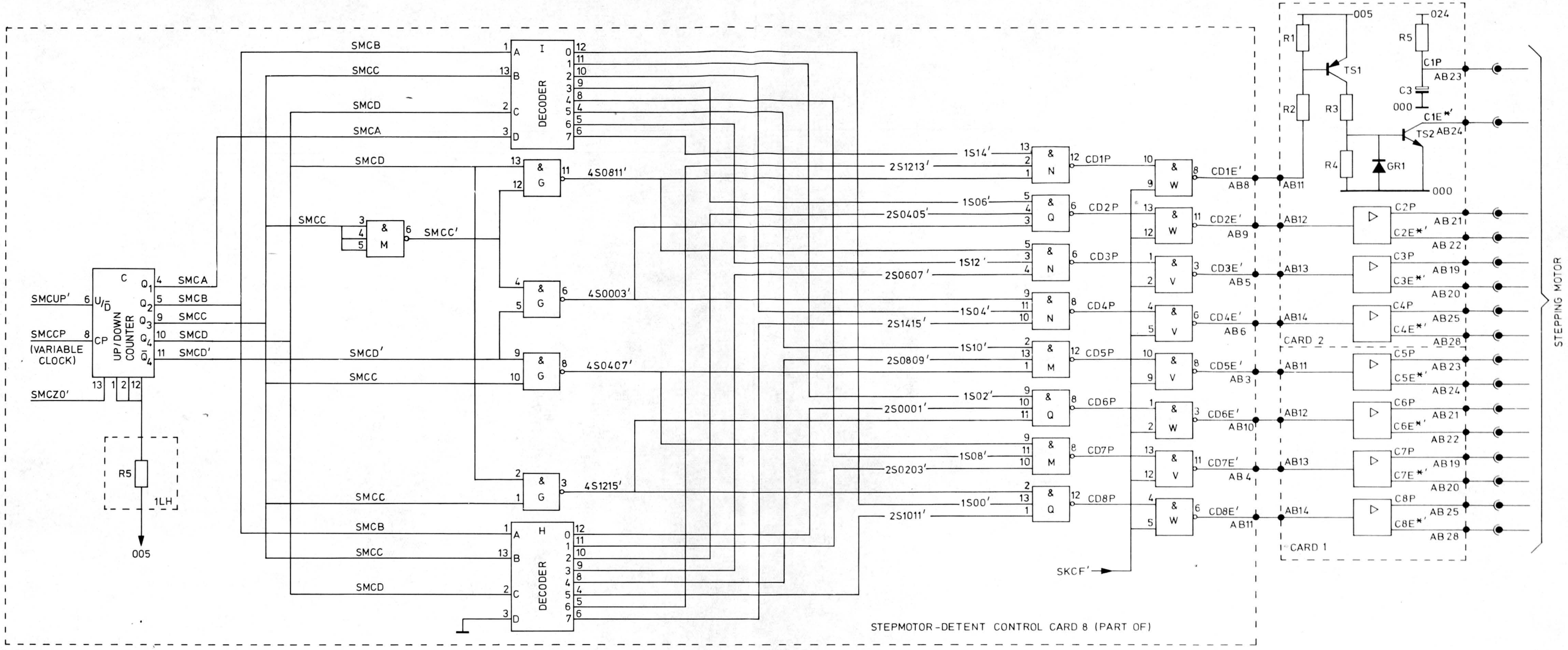
SDU- 20 SIGNAL-NAMES

SKFWD	SEEK DIRECTION FORWARD
SKFZ1	" -FF-SET
SKINH	" INHIBIT
SMCA	STEPMOTOR-COUNTER 2 EXP. 0
SMCB	" " 2 " 1
SMCC	" " 2 " 2
SMCCP	" " -CLOCKPULSE
SMCD	" " 2 EXP. 3
SMCEN	" " ENABLE
SMCUP	" " UP
SMCZO	" " RESET
SP	SECTOR PULSE
SPKF	SPEED OK-FF
SPKFZO	" " "-RESET
SPKFZ1	" " "-SET
SPKM	SPEED OK-MONOSTABLE
SPKMT1	" " " -TRIGGER 1
SPZ	" ZERO
SPZA	SECTOR PULSE
SSD	START-STOP-BUTTON DOWN
SSDF	" " " " -FF
SSU	" " " UP
STF	START-FF
STFZO	" "-RESET
STLØN	START-LAMP ON
STPF	STOP-FF
STPFZO	" "-RESET
STPFZ1	" "-SET

T000	TRACK 000
T204	TRACK 204
TAG1	TAGLINE 1
TAG1ZA	" 1
TAG2	" 2
TAG3	" 3
TBUS0	TEST BUSLINE 0
TBUS1	" " 1
TBUS2	" " 2
TBUS3	" " 3
TBUS4	" " 4
TBUS5	" " 5
TBUS6	" " 6
TBUS7	" " 7
TCP	TEST-CLOCKPULSE
TFF	TEST-FAST-FF
TFWD	TEST FORWARD
TREV	TEST REVERSE
TSKINH	TEST SEEK INHIBIT
TSW	TEST SWITCHES
TTAGIM	TEST TEST-TAGLINE 1 MONOSTABLE

SDU 20 SIGNAL-NAMES

US	UNSAFE
USF	" -FF
USFL0N	" LAMP ON
USFZ1	UNSAFE-FF-SET
USFZA	UNSAFE FF
USFZB	" "
WRDA	WRITE DATA
WRDAZA	WRITE DATA
WREN	" ENABLE
WRER	" OR ERASE ENABLE



UP/DOWN COUNTER OUTPUTS					DECODER INPUTS				DECODER OUTPUTS								4S1215'	4S0811'	4S0407'	4S0003'	STEPPING MOTOR COIL DRIVER INPUTS							
Q1	Q2	Q3	Q4	$\bar{Q}4$	A	B	C	D	0	1	2	3	4	5	6	7					CD1E'	CD2E'	CD3E'	CD4E'	CD5E'	CD6E'	CD7E'	CD8E'
0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0
1	0	0	0	1	0	0	0	0 \ 1	0 \ 1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	1
0	1	0	0	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	0	1
1	1	0	0	1	1	0	0	0 \ 1	1	0 \ 1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	0	1
0	0	1	0	1	0	1	0	0	1	1	0	1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	0	1
1	0	1	0	1	0	1	0	0 \ 1	1	1	0 \ 1	1	1	1	1	1	1	1	0	1	1	0	1	1	0	1	0	1
0	1	1	0	1	1	1	0	0	1	1	1	0	1	1	1	1	1	1	0	1	1	0	0	1	0	1	0	1
1	1	1	0	1	1	1	0	0 \ 1	1	1	1	0 \ 1	1	1	1	1	1	1	0	1	1	1	0	1	0	1	0	1
0	0	0	1	0	0	0	1	0	1	1	1	1	0	1	1	1	1	0	1	1	0	1	0	1	0	1	0	1
1	0	0	1	0	0	0	1	0 \ 1	1	1	1	1	0 \ 1	1	1	1	1	0	1	1	0	1	0	1	0	1	1	1
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0	1	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	0	1	1	1	0	1	1	0	1	0	1	0
1	1	1	1	0	1	1	1	0 \ 1	1	1	1	1	1	1	1	0 \ 1	0	1	1	1	1	1	1	0	1	0	1	0

NOTE
TABLE SHOWS CONDITIONS FOR DECODERS H & I THUS:

H \ I = 0 \ 1

FIG. 3·5- THE DECODING LOGIC

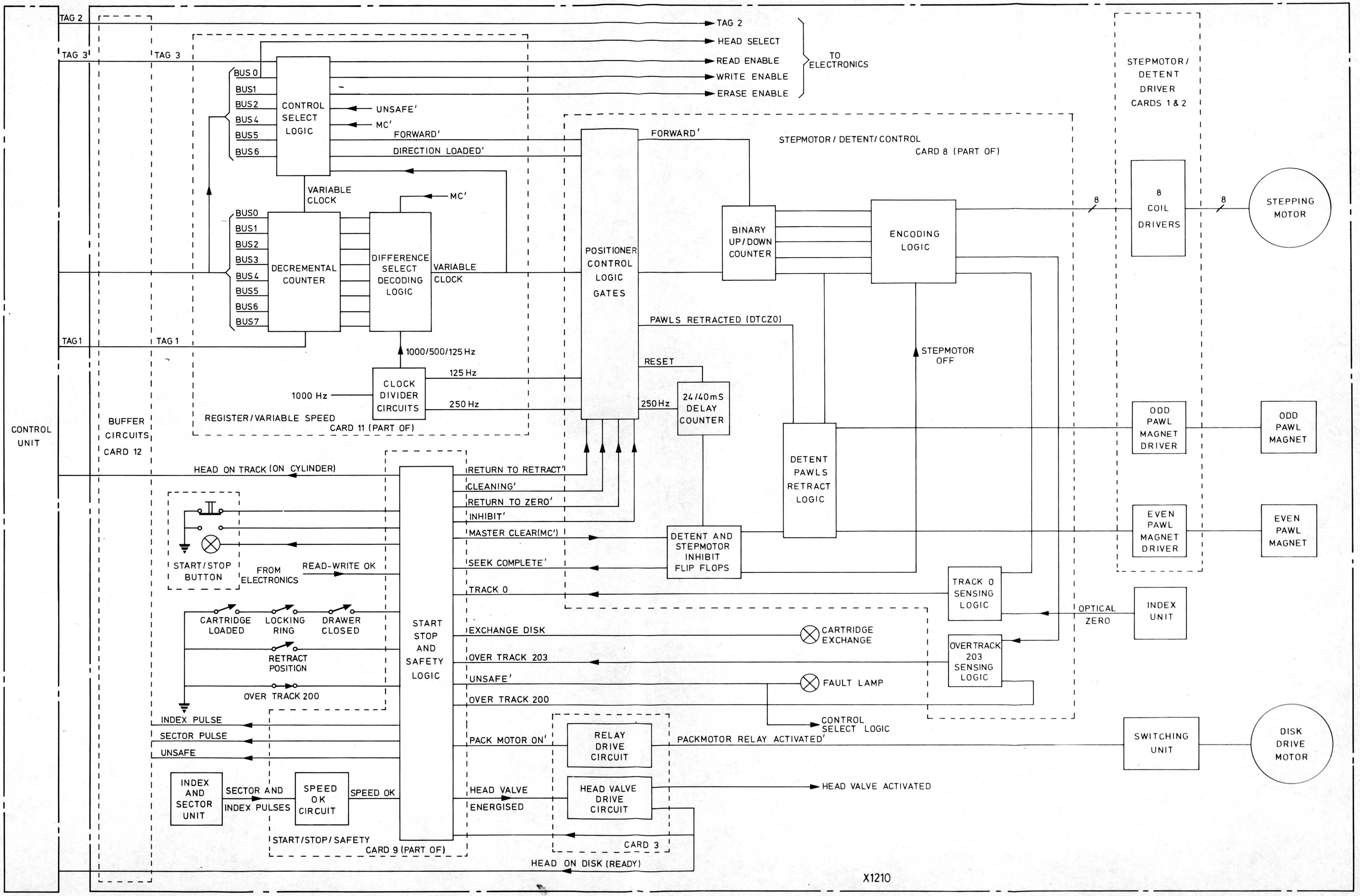


FIG. 3·8- BLOCK DIAGRAM OF X1210 LOGIC

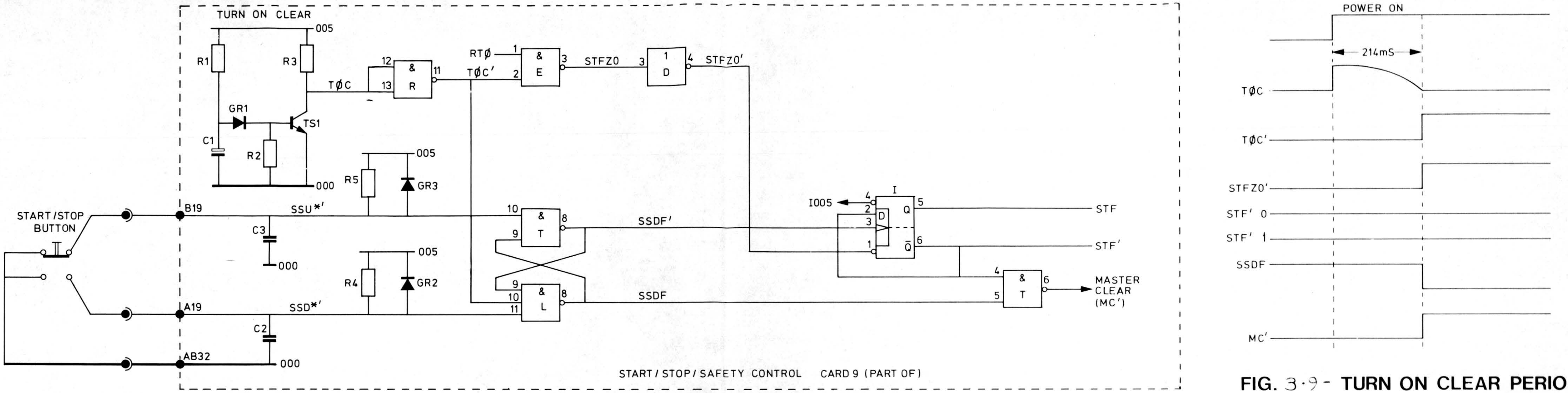


FIG. 3·9 - TURN ON CLEAR PERIOD

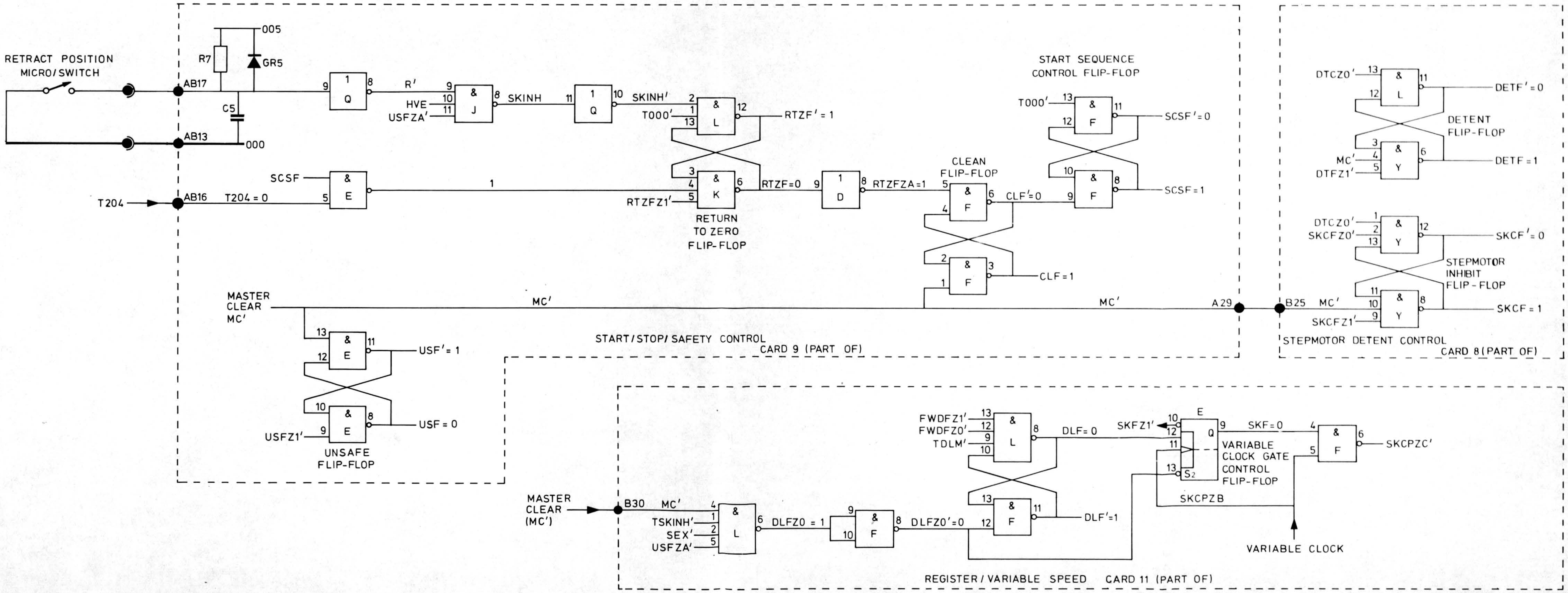
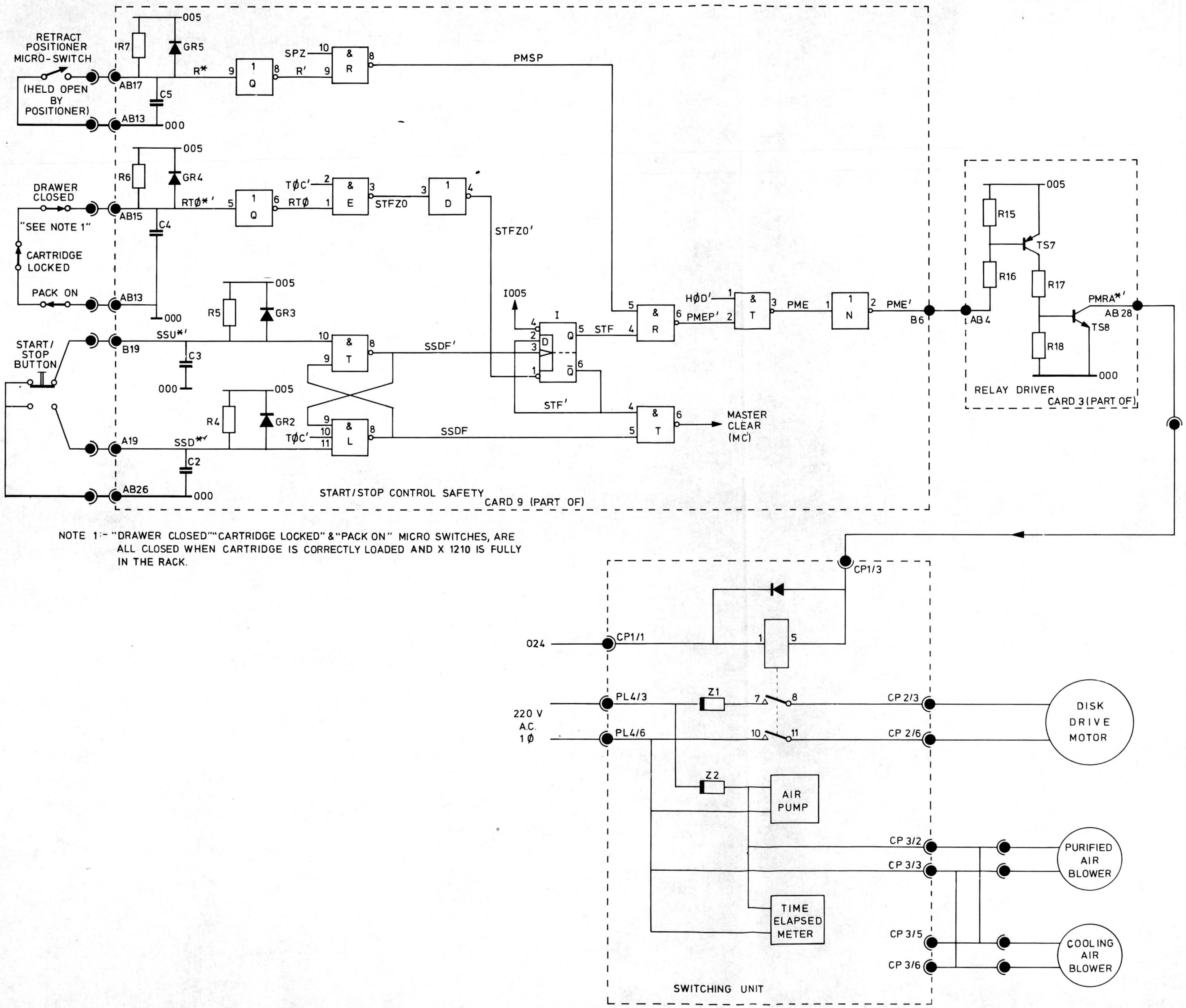
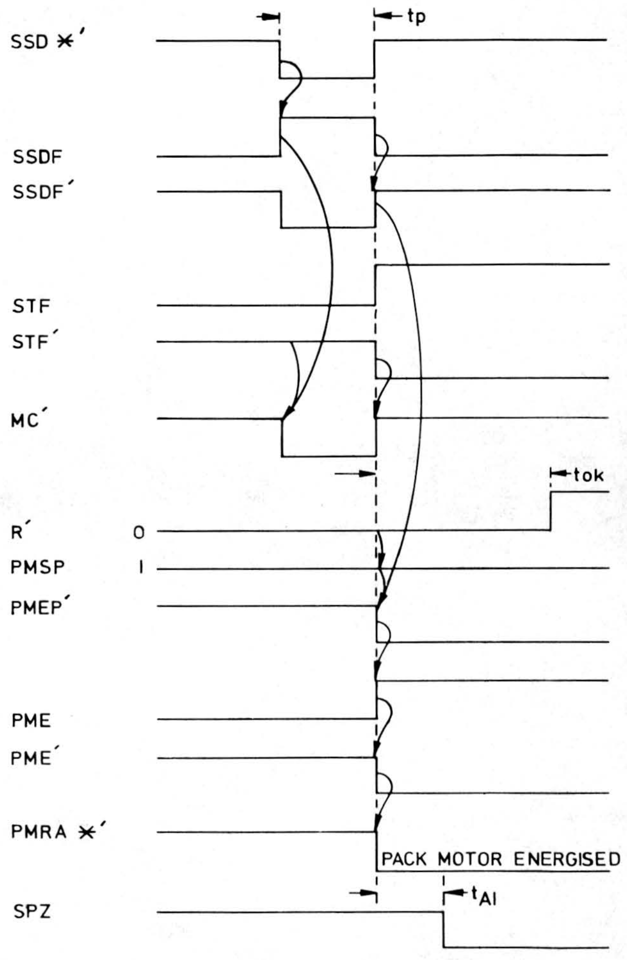


FIG. 3·10 LOGIC CONDITIONS SET BY MASTER CLEAR



NOTE 1:- "DRAWER CLOSED" "CARTRIDGE LOCKED" & "PACK ON" MICRO SWITCHES, ARE ALL CLOSED WHEN CARTRIDGE IS CORRECTLY LOADED AND X 1210 IS FULLY IN THE RACK.



X1210 START WAVEFORMS.

NOTE. tp = DURATION START/STOP BUTTON IS PRESSED.
t_{AI} = ROTATIONAL DELAY + CIRCUIT DELAY.
(SEE VOLUME 5)
tok = TIME FOR DISK TO REACH FULL SPEED.

FIG. 3·11 STARTING THE X1210

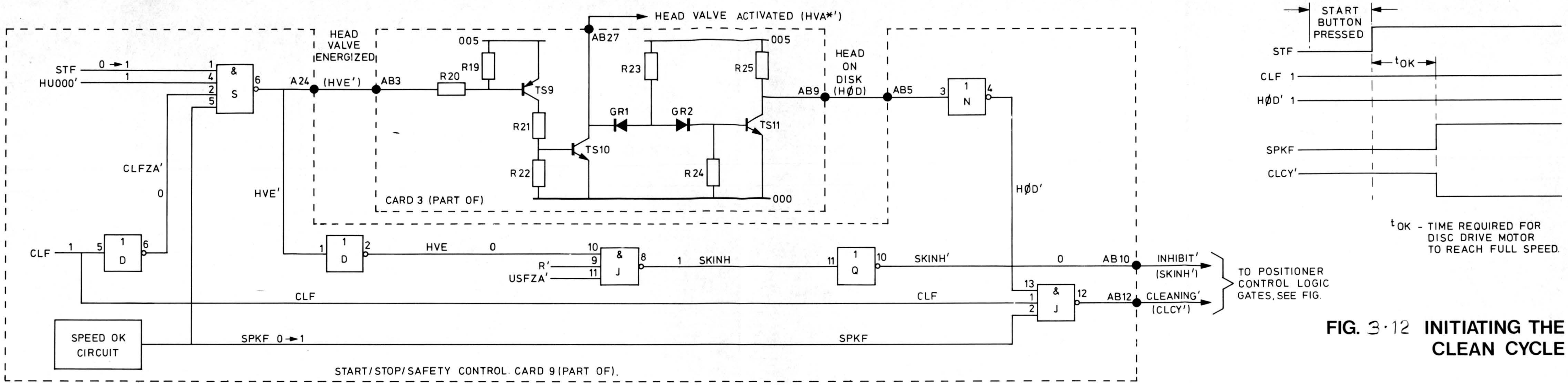


FIG. 3·12 INITIATING THE CLEAN CYCLE

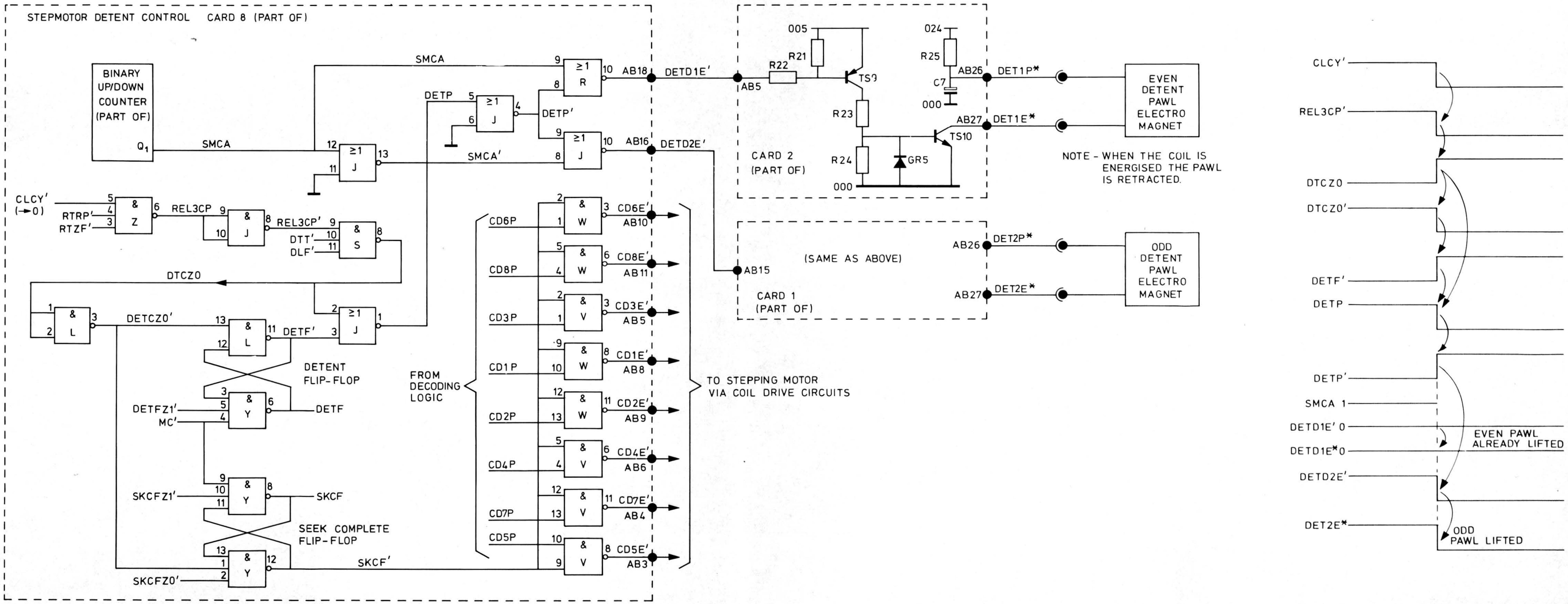


FIG. 3·13 PAWLS RETRACTED/ STEPMOTOR DRIVE CIRCUITS ENABLED

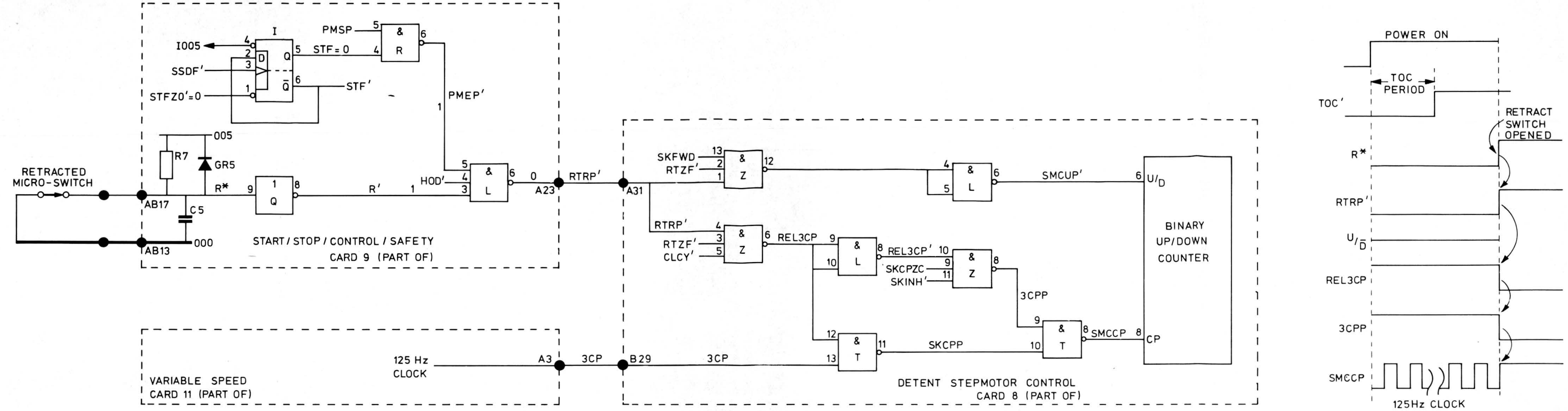


FIG. 3·14 TOC PERIOD - POSITIONER NOT FULLY RETRACTED

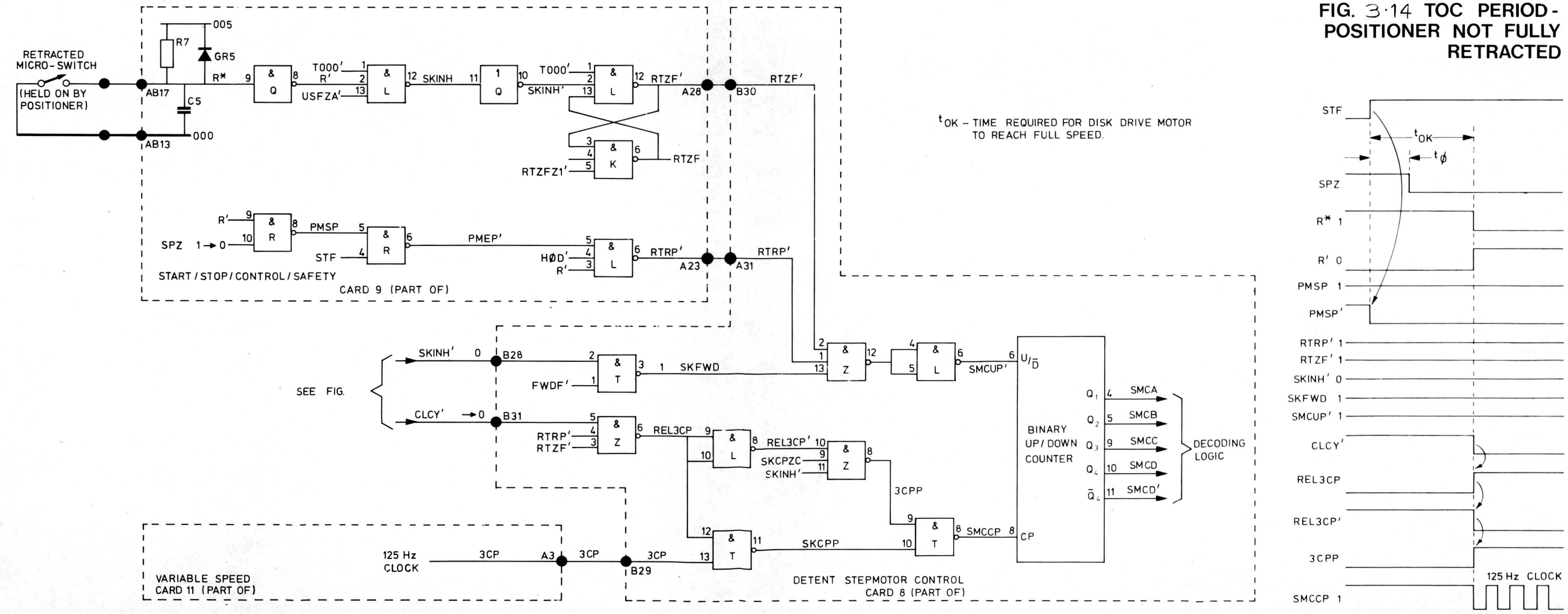
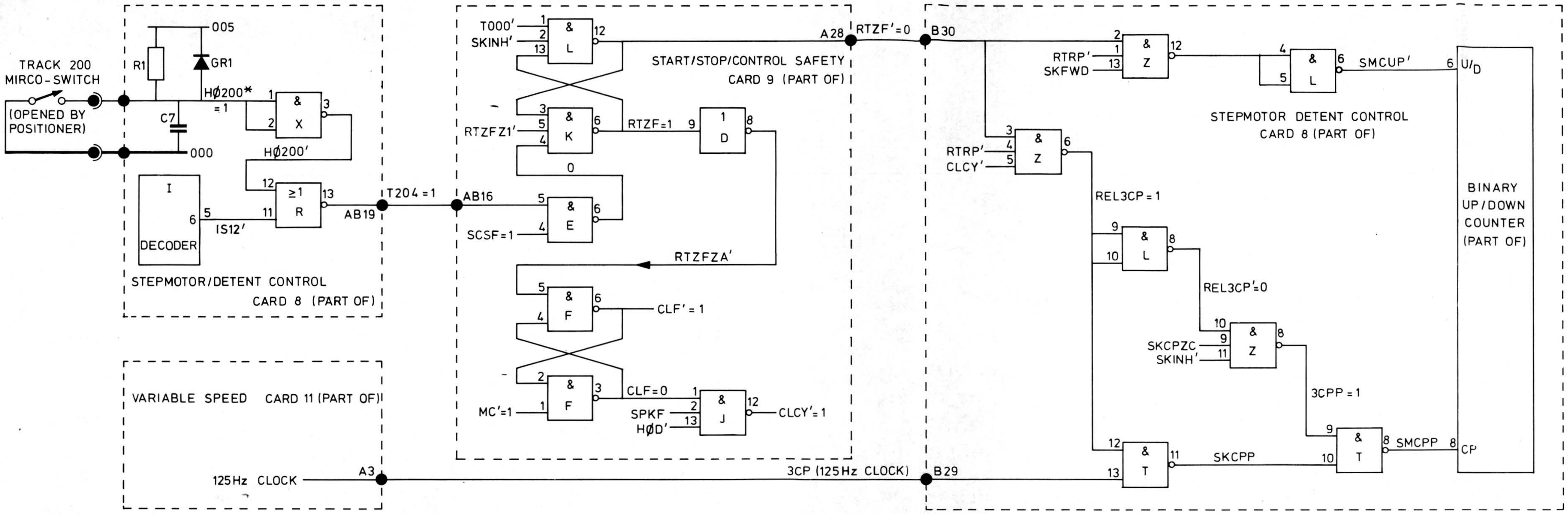


FIG. 3·15 CLEANING CYCLE - MOVING FORWARD INTO THE CARTRIDGE



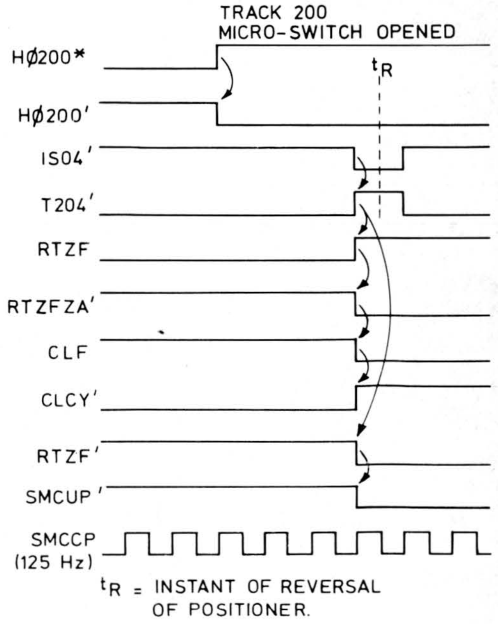
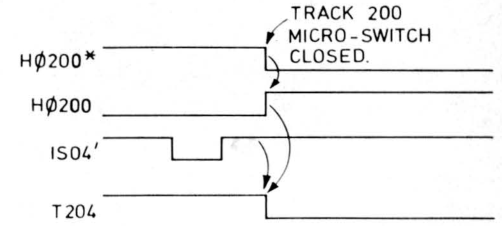
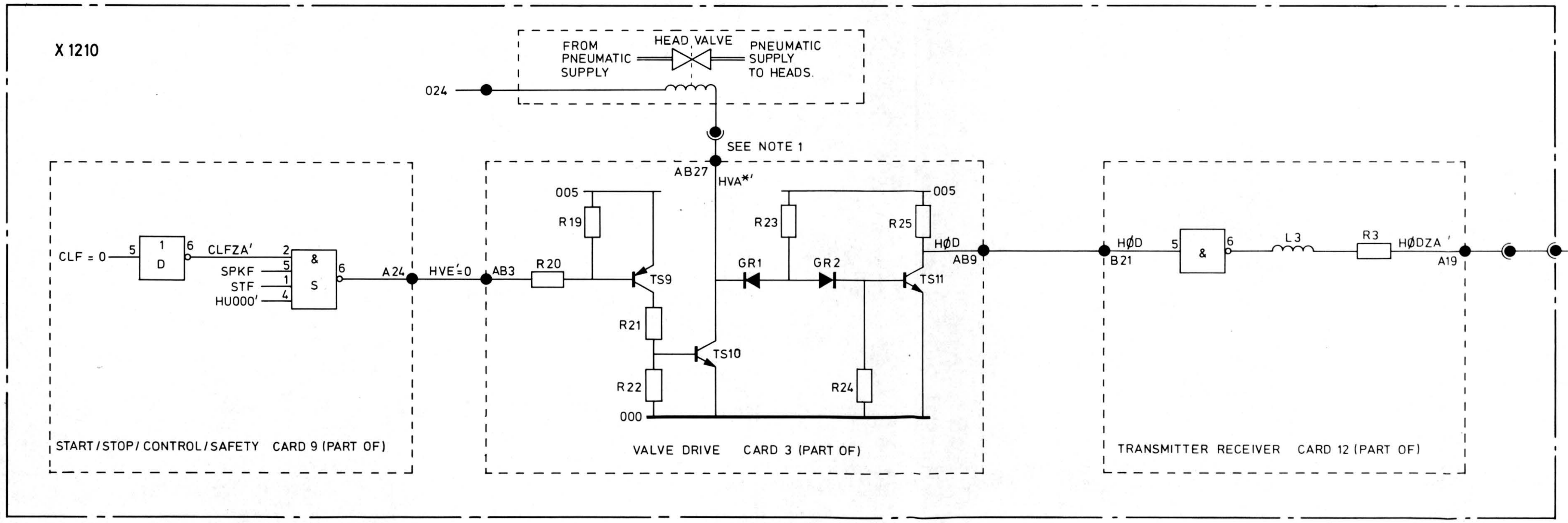


FIG. 3·16 END OF CLEAN CYCLE/ REVERSAL AT TRACK 204

NOTE 1 - WHEN HVA*' = 0, THE HEAD VALVE OPENS AND APPLIES THE PNEUMATIC SUPPLY TO THE HEAD ASSEMBLIES.



EVENTS OCCURING SHORTLY AFTER REVERSAL AT T200



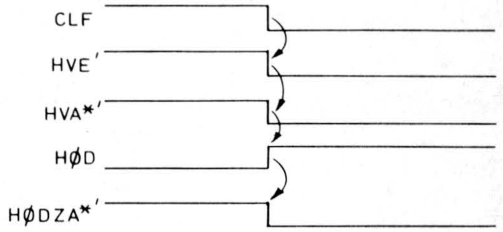
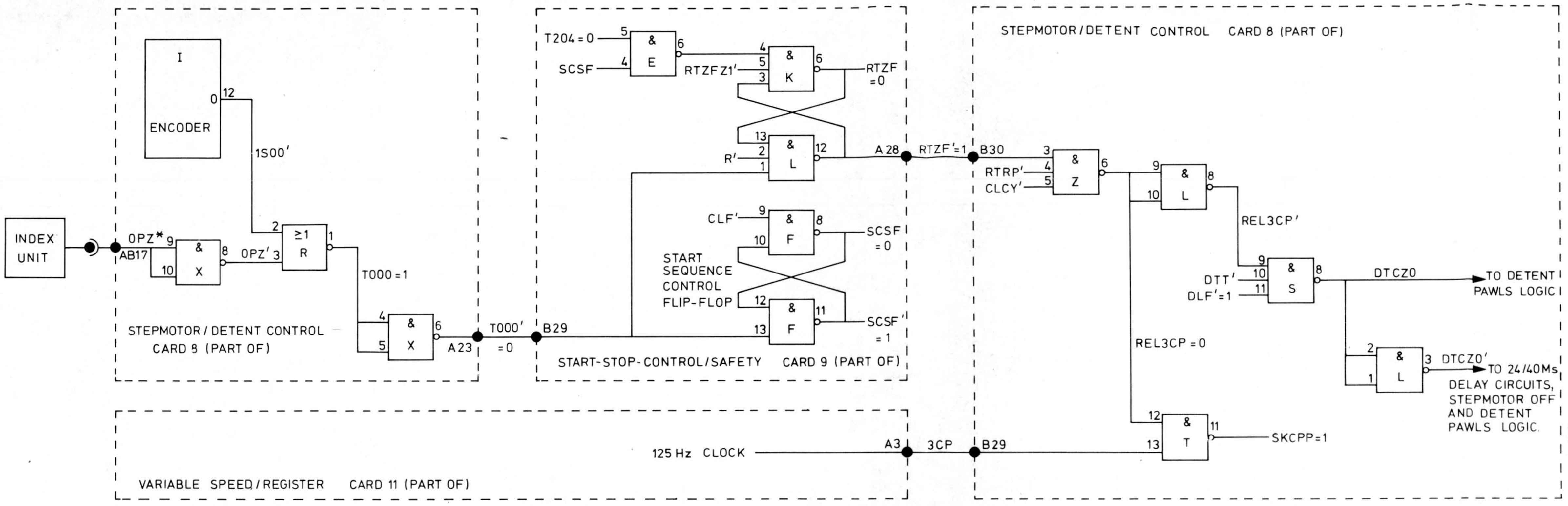


FIG. 3·17 ENERGISING THE HEAD VALVE



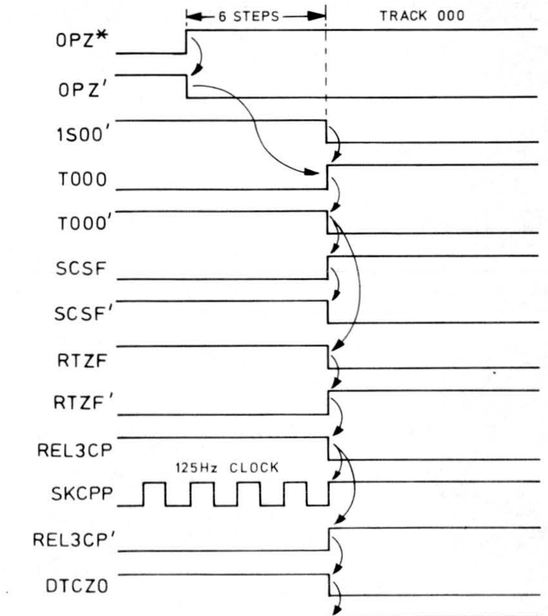


FIG. 3-18 SENSING TRACK 000/ INITATING DELAY, DETENT & STEPMOTOR OFF LOGIC.

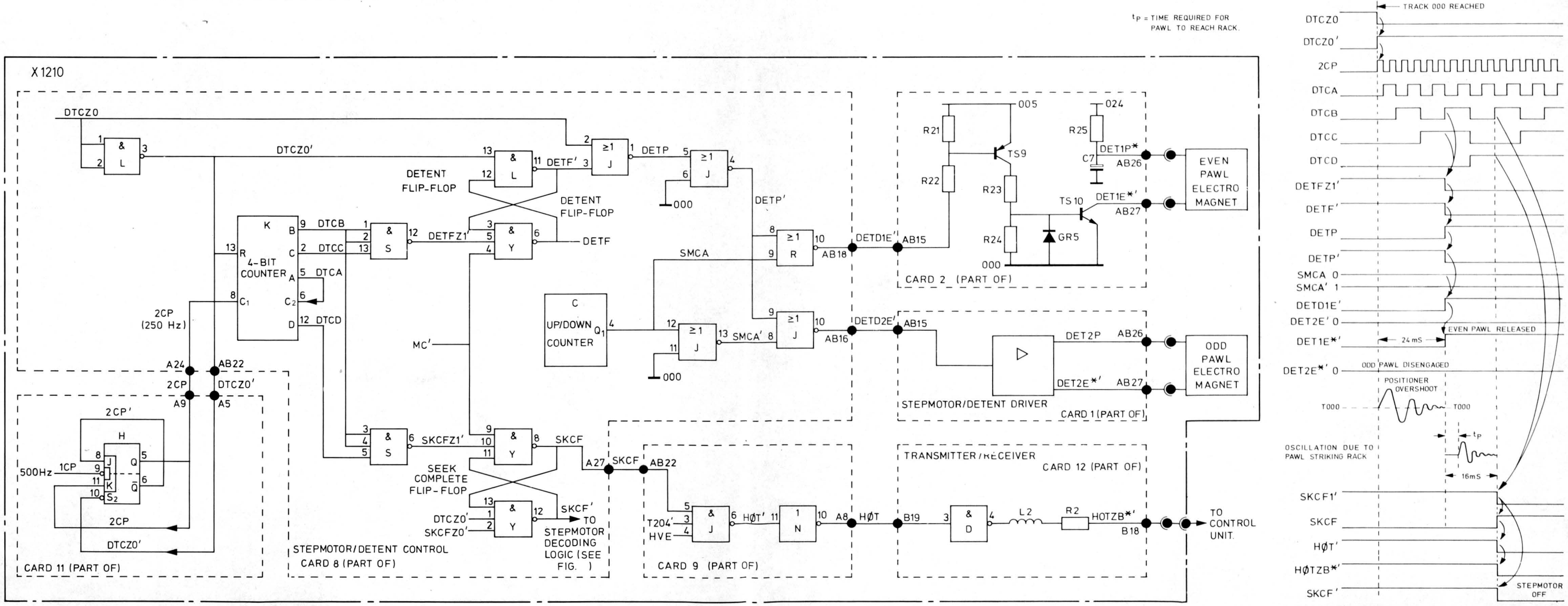


FIG. 3-19 24/40ms DELAY CIRCUIT, DETENT AND STEPMOTOR INHIBIT LOGIC OPERATION

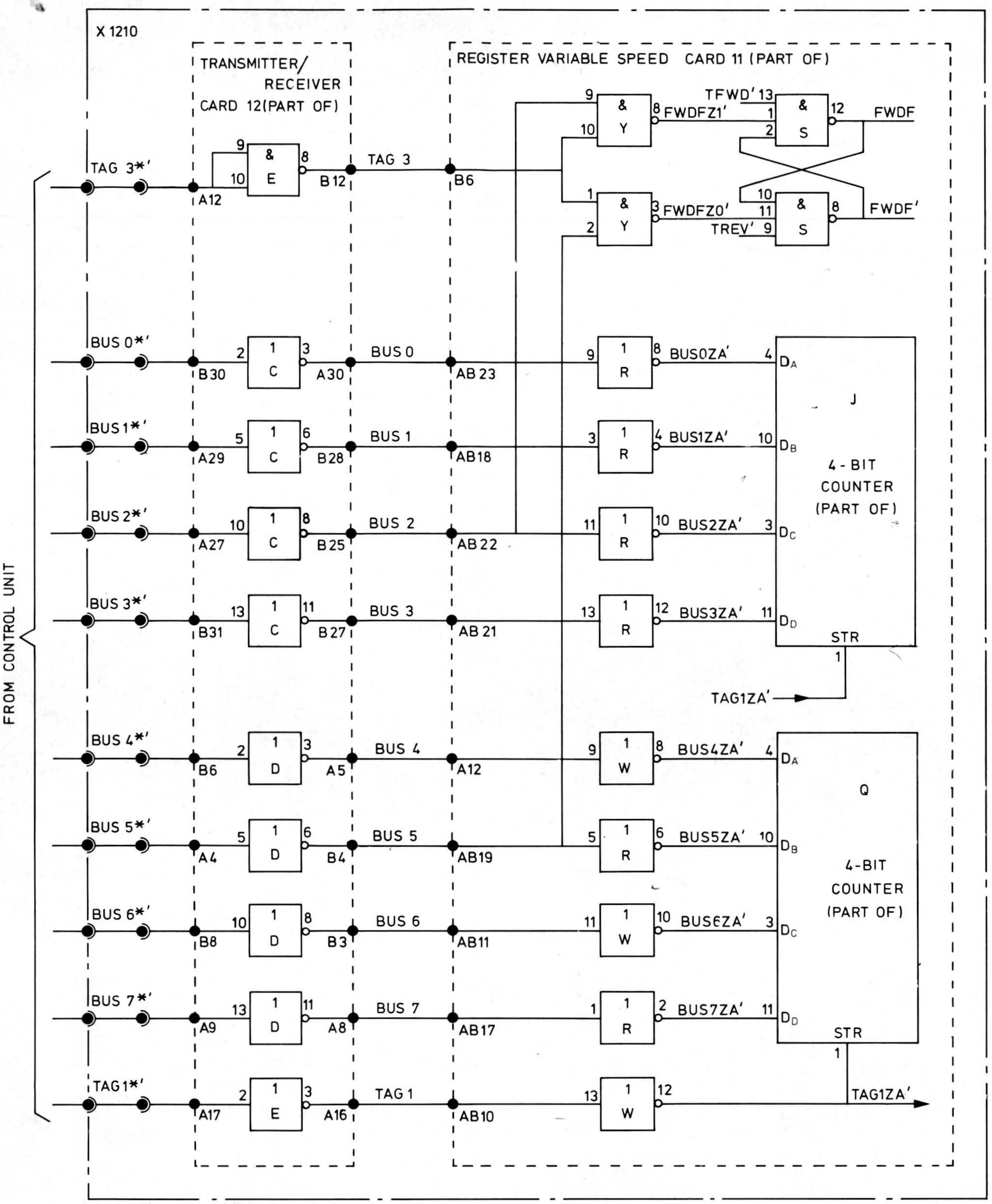


FIG. 3·27 INTERFACE POSITIONING INSTRUCTIONS

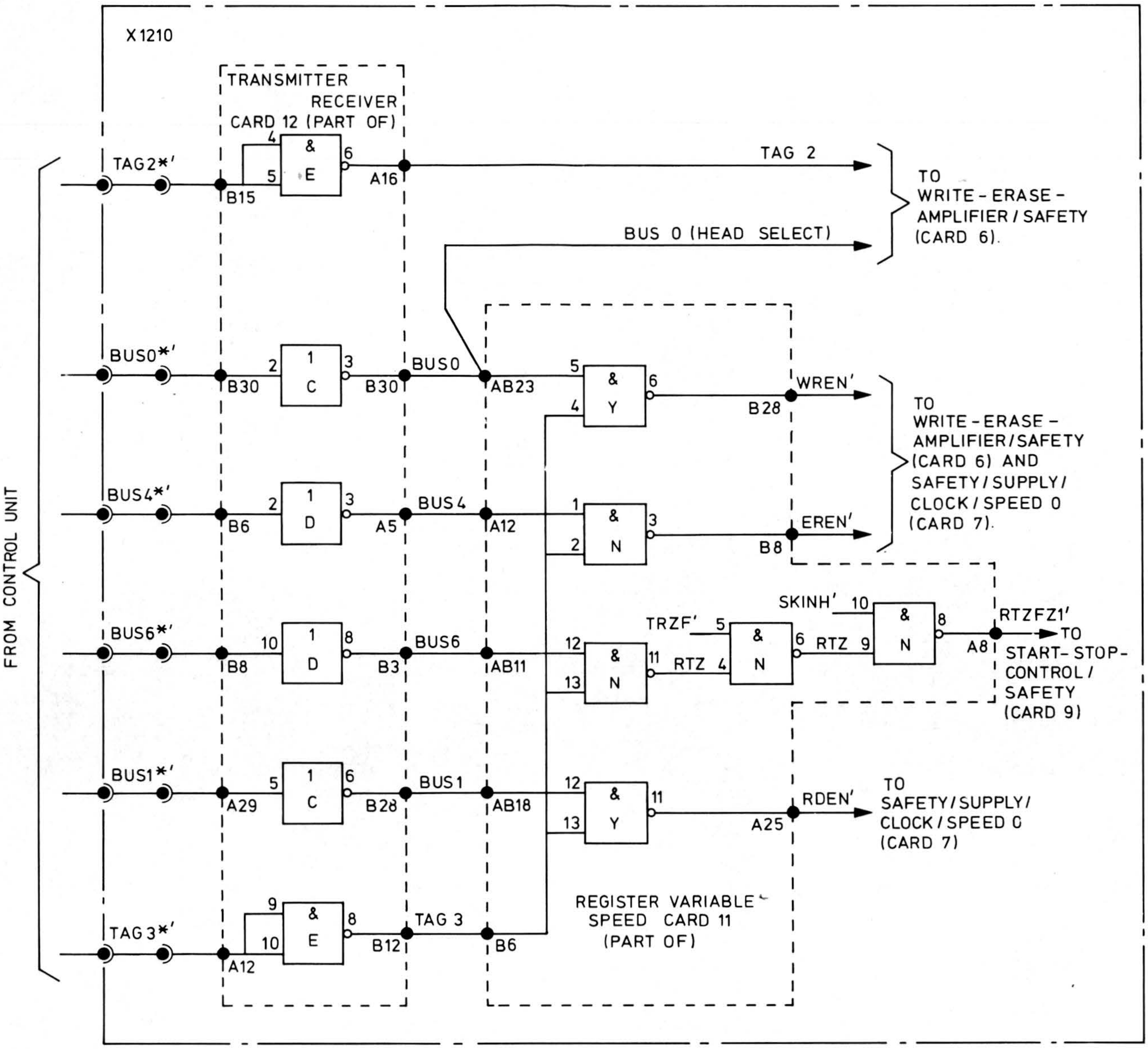


FIG. 3·28 INTERFACE CONTROL SELECT INSTRUCTIONS

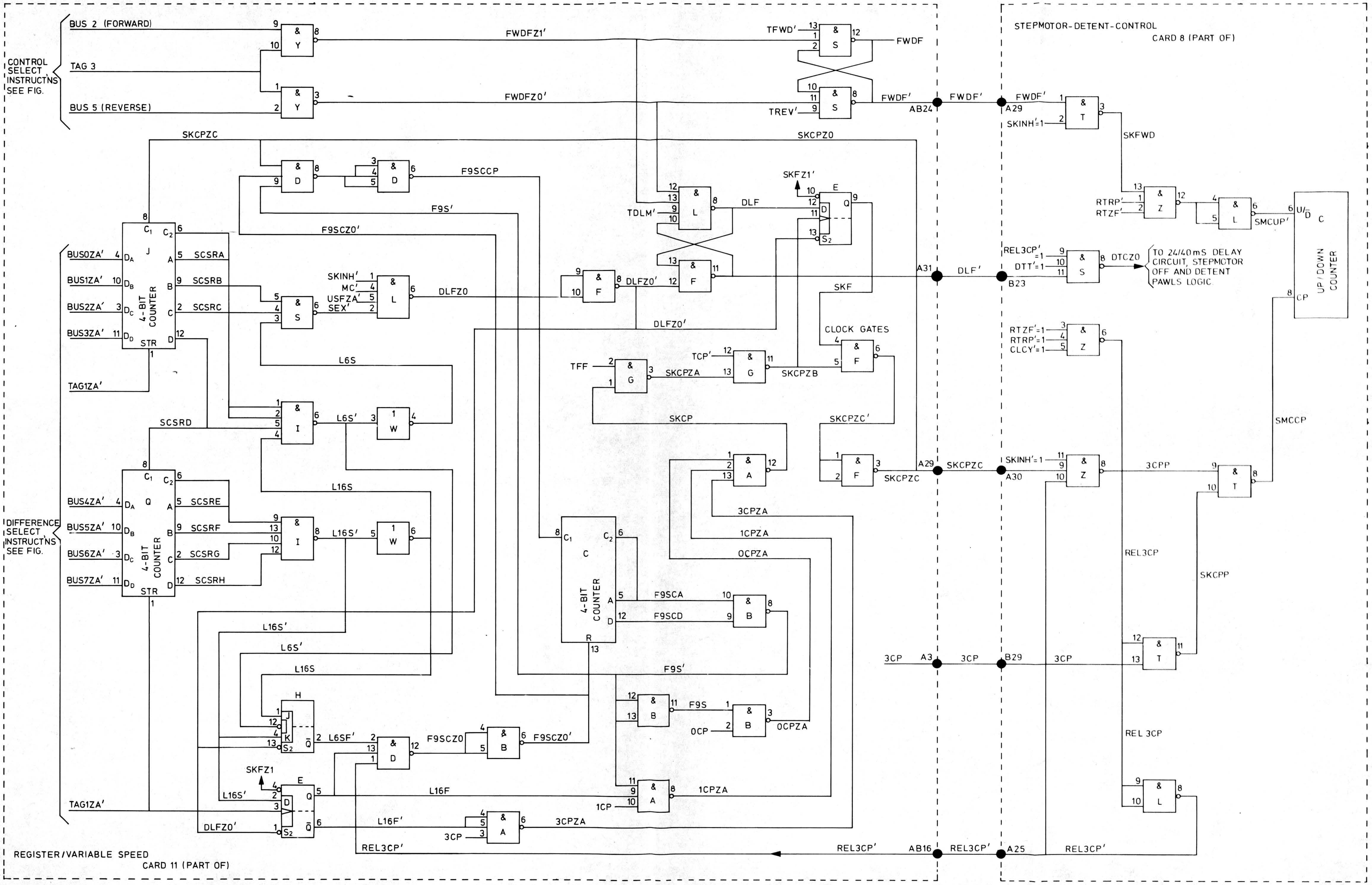


FIG. 3·29 SEEK MISSION OF GREATER THAN 16 STEPS

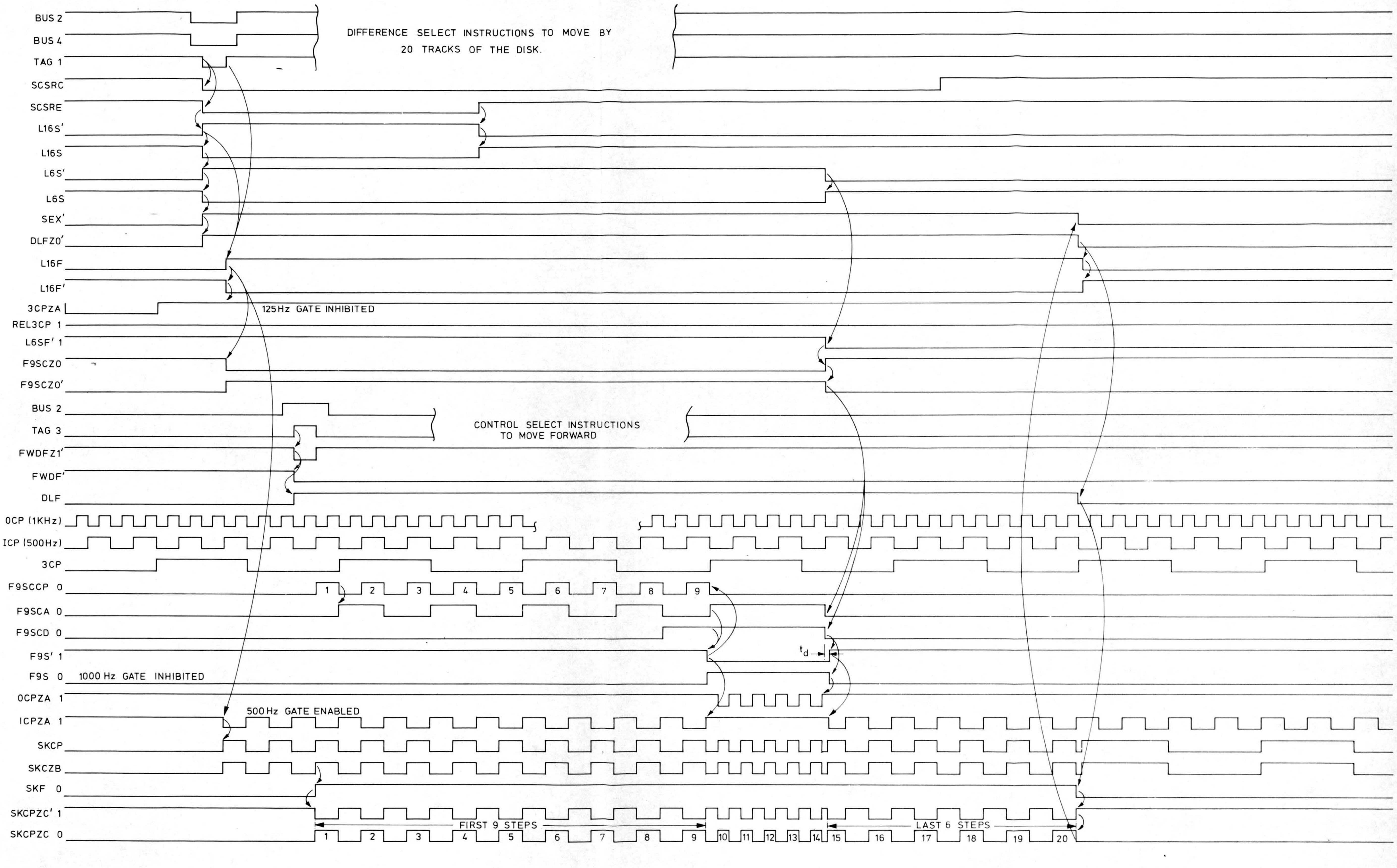


FIG. 3·30 SEEK MISSION OF GREATER THAN 16 STEPS

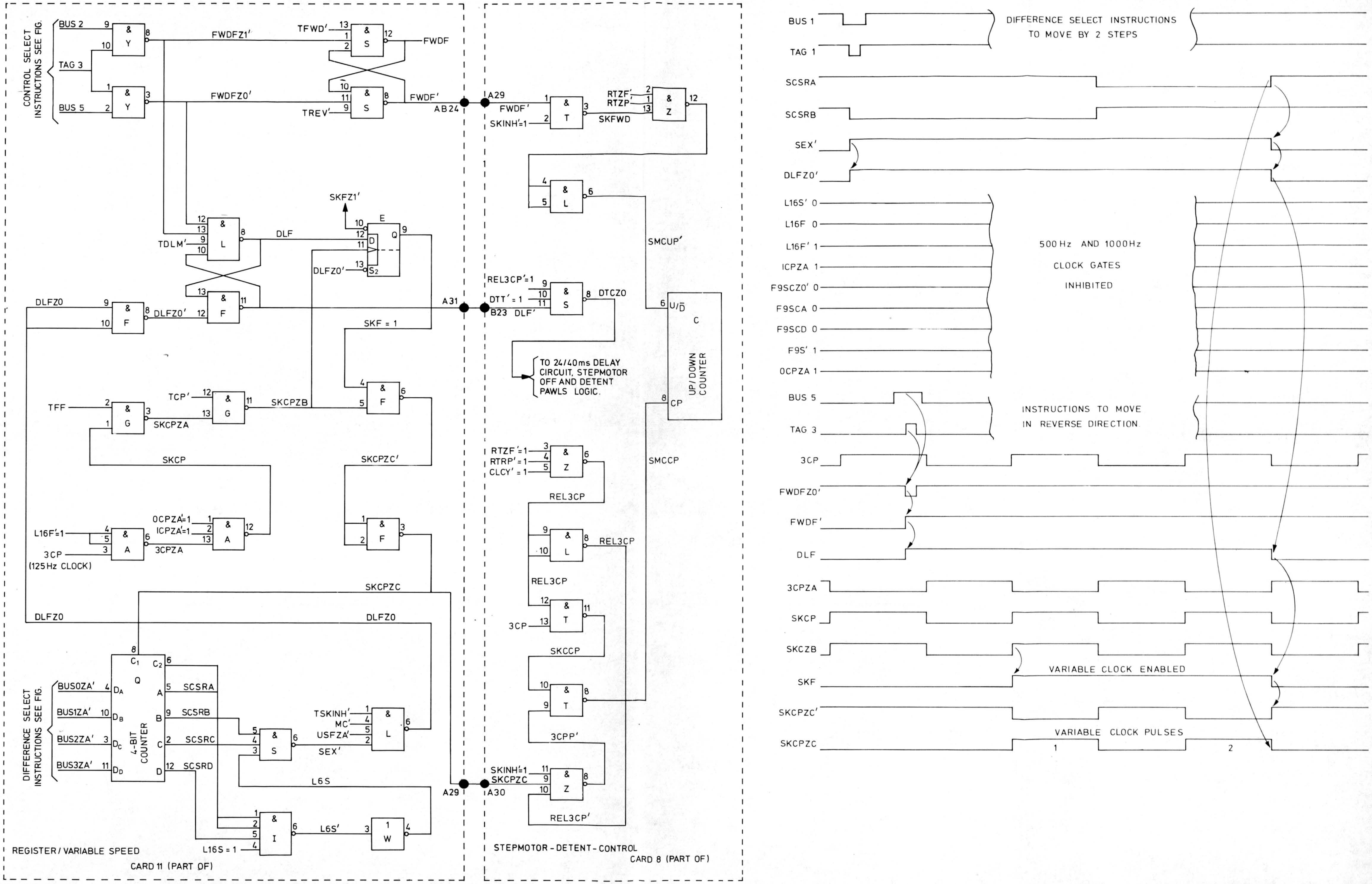
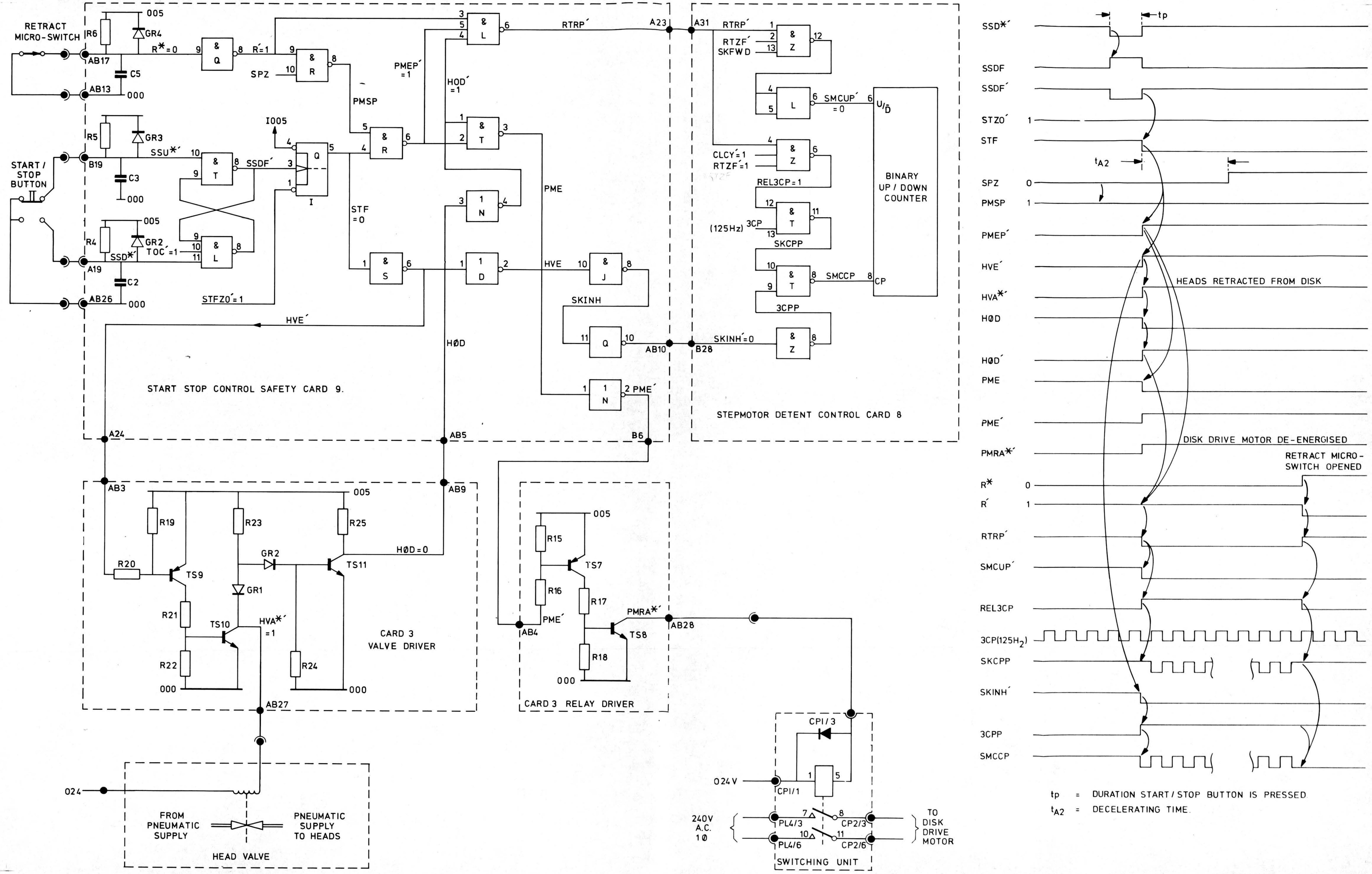


FIG. 3·34 SEEK MISSION OF LESS THAN 16 STEPS



tp = DURATION START / STOP BUTTON IS PRESSED.

t_{A2} = DECELERATING TIME.

FIG. 3·35 STOPPING THE X1210